CMOS Buffer Tapering with Interconnect Capacitances

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ABSTRACT

The equations for optimal tapering are derived for CMOS buffers which take account of the interconnect capacitance between stages. This extends existing results to the design of signal distribution networks.

1. Introduction

The quest for the optimum tapering factor of a chain of CMOS buffers has been well reported. Jaeger[1] established in 1975 that the optimum fixed tapering factor for minimum delay was e based upon a simple RC delay characterization. This was refined in 1987 by Hedenstierna and Jeppson[2] using transistor equations, in 1990 by Li *et al* [3] who split the output and input buffer capacitances, and in 1992 by Prunty and Gal[4] with the inclusion of short-circuit current effects. The idea of a variable-taper was introduced in 1991 by Vemuru and Thorbjornsen[5] to reduce the total area with minimal increase in delay; and similarly used in 1994 by Ma and Franzon [6] to reduce energy consumption. In 1994, Choi and Lee[7] derived a fixed tapering factor to minimize the power-delay product. A unified treatment of much of this work was presented in 1995 by Cherkauer and Friedman[8].

In generating signal (and particularly clock) networks, the buffer-sizing problem is affected by the interconnect capacitances of the distribution net. This letter examines the effect of these on the optimum tapering factor using the original RC model (without split capacitors), and looks briefly at possible applications in CAD-tool development.

2. Buffer chain delay

We examine the following problem: given a fixed number of buffers with a known set of interconnect capacitances between each stage, what tapering factors achieve minimum delay?

Suppose the buffer cascade consists of $n+1$ buffers (numbered 0 to n) with interconnect capacitances I_i (i: 0→n) such that I_i is driven by buffer(i). Let W_i be the total width of the buffers at level i with W_0 fixed and W_{n+1} having the equivalent capacitance to the final load which the network drives. At each level of the network, there may be several independent buffers; however, we consider only the sum of their widths. Finally, let C_i be the total capacitance driven by the buffers at level i.

If the buffers all have the same gate length, then can assume that their input capacitance and their drive capability are both proportional to their width. Thus the delay of the buffers at level i is proportional to C_i/W_i and:

$$\text{Total Delay} \propto \sum_0^n \frac{C_i}{W_i} \propto \sum_0^n \frac{W_{i+1} + I_i}{W_i}$$

Since W_0, W_{n+1} and I_i (i: 1−> n) are fixed, the above is a function in W_i (i: 1→n). To find a stationary point, we set the partial derivatives to zero giving;

$$\frac{1}{W_{i-1}} - \frac{W_{i+1} + I_i}{W_i^2} = 0$$

The matrix of second partial derivatives (the Hessian matrix) can be shown to be positive definite which implies that the stationary point is a minimum. If we define f_i to be equal to the ratio of the widths of successive buffers (the tapering factor) then:

$$f_i = \frac{W_i}{W_{i-1}} = \frac{W_{i+1} + I_i}{W_i} = f_{i+1} + \frac{I_i}{W_i}$$

gives minimum delay with the restriction that W_0 and W_{n+1} are fixed. Notice that this leads to a variable tapering factor; f_i is constant only if $I_i = 0$ for all i.

The main points are that for optimal speed the sequence of tapering factor $\{f_i\}$ is *monotonically decreasing* along the buffer chain, and that the decrease is the ratio of the interconnect capacitance to the width of the preceding buffer, as illustrated in figure 1. One interesting consequence is that if the final stages have a high interconnect capacitance, then the final tapering-factors may be less than one (i.e. the buffer width may decrease in the final stages), as shown in figure 2.

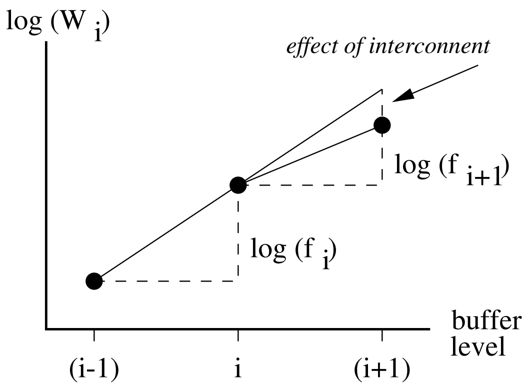

Fig. 1. Effect of interconnect capacitance on optimal widths

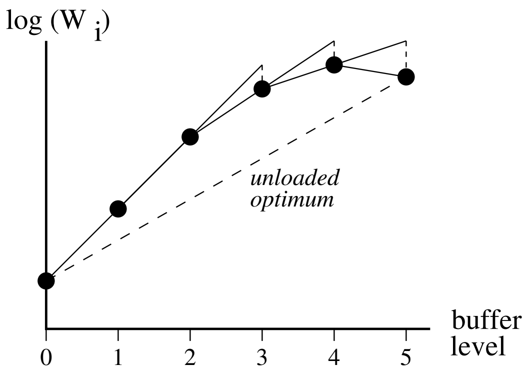

Fig. 2. Optimal buffer sizes with interconnect capacitance

3. Application area

With a known interconnect and load capacitance, the above equation can be used to optimized buffers sizes. This may be used in a CAD environment where the final clock buffer sizes are chosen after layout to remove skew due to routing-dependent capacitances in standard-cell systems[9]. Alternatively, with a routing capacitance estimator, the equation can be used to explore different clock distribution architectures and so determine the most appropriate number of buffers and distribution strategy for a specific design.

4. Conclusions

We have extended the simple model for CMOS buffer-chain delay to include interconnect capacitance, for application in signal-distribution design. The result is that for minimum delay the tapering-factor is variable and monotonically decreasing along the buffer chain.

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