EE 4743/6743
Lab1 : Intro to Schematic Capture/Simulation with Maxplus2

Objective:

The objective of this lab is to become familiar with schematic capture and simulation using the Altera Maxplus2 toolset.

To Do:

You are to create two schematics, *reg1bit* and *reg4bit*. These schematics are shown on following page. Reg1bit implements a 1-bit register, and reg4bit uses four copies of reg1bit to implement a 4-bit register. Duplicate both the schematics and waveforms shown on the following pages and demonstrate your completed work to the Lab TA. When editing the waveform, you will need to use "Options" → "Grid Size" to set the grid size to 1.0 ns. Attempt to duplicate the input wavesforms as close as reasonably possible (the clock period is 20 ns; changes in LOAD, DIN should occur at least 2 ns after the rising clock edge; make the low pulse width on RESET_B at least 3 ns).

a. Do three simulations of the reg1bit waveform. For the first simulation, after the schematic is created, select the compiler via "MAX+plus II" → "Compiler" , then use the "Processing" menu and select "Functional SNF Extractor" (checkmark should appear) to select simulation with no timing information. Compile the schematic and simulate (this should produce the output waveforms shown on the next page assuming you have the input waveforms as shown). Make sure that you create a screen capture of this waveform.
b. For the 2nd simulation, the use the "Processing" menu to UNSELECT "Functional SNF Extractor" – a checkmark should appear by "Timing SNF Extractor". Then use the "Assign" → "Device" menu to assign a Family = MAX 7000, Device = Auto and re-compile, resimulate. This map the design to a Max 7000 PLD and use timing values from that device. Make sure that you create a screen capture of this waveform.
c. For the 3rd simulation, assign the device to be Family = Flex10K, Device = Auto and recompile, resimulate. Make sure that you create a screen capture of this waveform.
d. For the reg4bit schematic, you only need to do one simulation, with 'Functional SNF Extractor" checked.

Questions:

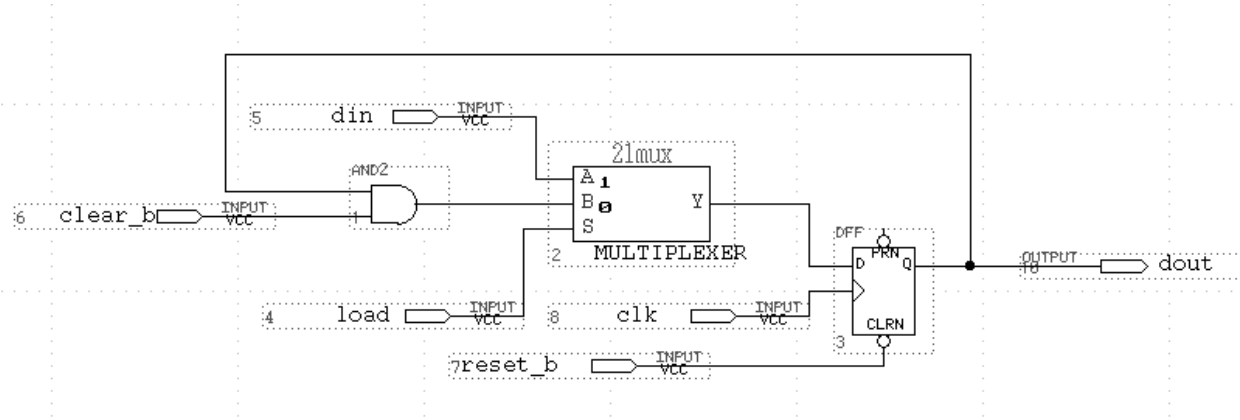
a. In the REG1BIT simulations,what changes do you see between the simulations with the 'Functional SNF Extractor' option checked versus the 'Timing SNF Extractor' option checked. Relate your answer to timing parameters on the components within the REG1BIT schematic.

b. In looking that the REG1BIT simulations for the Max7000 device versus the Flex10K device, which is the slower device? Defend your answer by referencing points on the two waveforms. From the two waveforms, give the Clock-to-Dout delays of the REG1BIT design in the Max7000 family versus the Flex10K family.

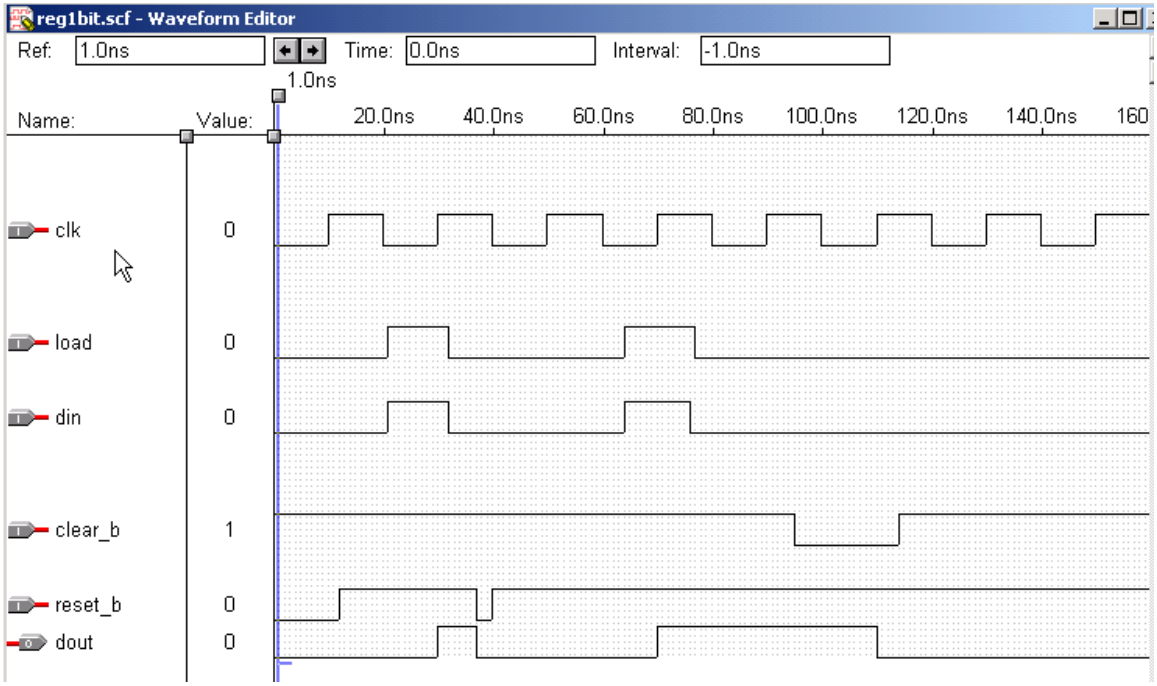
c. Is the reset input a synchronous or asynchronous input? Defend your answer by referencing the simulation waveforms.

d. Is the clear_b input a synchronous or asynchronous input? Defend your answer by referencing the simulation waveforms.

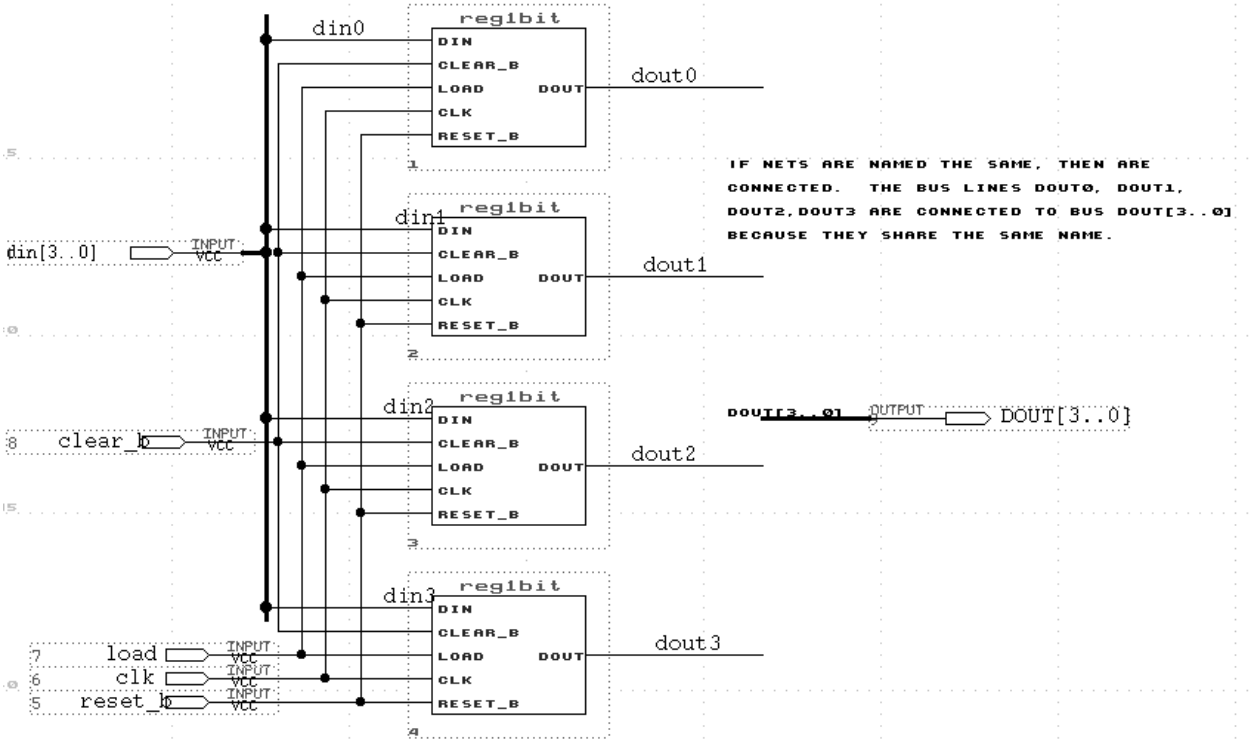
Reg1bit



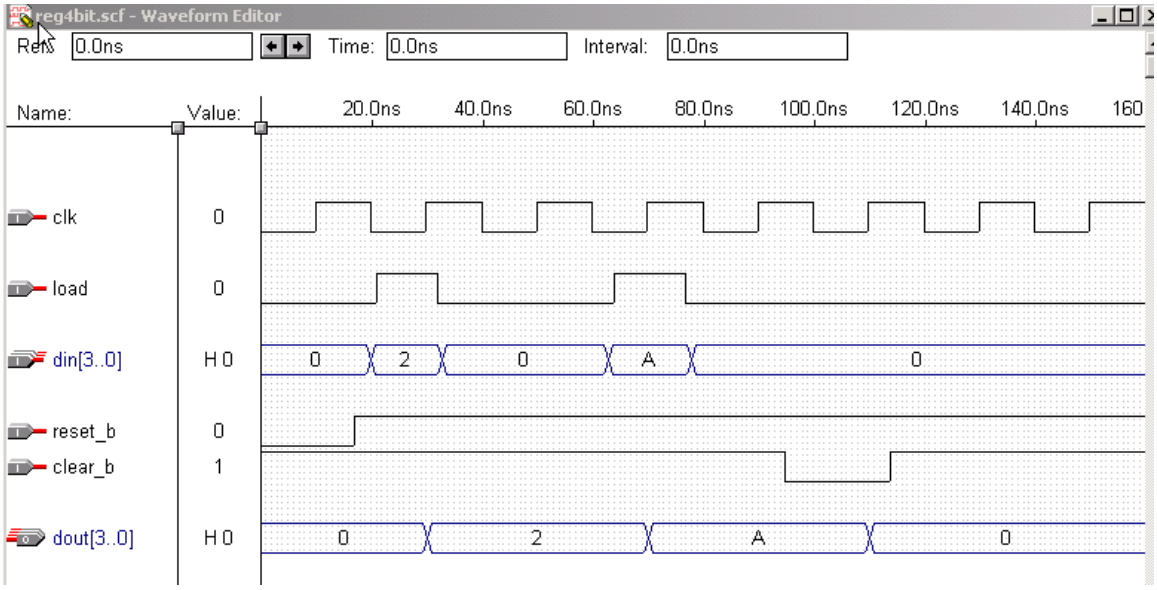
REG1BIT Simulation



Reg4bit Schematic



Reg4bit Simulation



Tips On Schematic Capture

1. Use File -> New Graphic Editor File (GDF) to create a new schematic.
2. Double clicking on white space in the schematic will bring up the dialog box that allows you add new components. This lab uses components from the 'max2lib/prim' and 'max2lib/mf 'libraries. The component names used in this schematic are AND2, 21MUX (mf library), DFF, INPUT (input pin), OUTPUT (output pin)
3. To add a net (connection) between two components, click on the pin and drag to make a connection to another pin.
4. To label a pin, click on the name and type in text. To label a net, click on the net and add the text.
5. The 'compile' step is necessary before simulating your schematic. Use the File -> Project -> Save & Compile.
6. If you have multiple schematics open, to compile the current schematic, you must use Project -> Set project to current file before using the Save & Compile command.
7. To create a bus, you can use the 'line type' selector in the upper right corner of the menu to select a wider line style, then click on the 'line' draw symbol along the left hand side before drawing the line. The line style is ONLY for aesthetic purposes only; a bus is identified by its NAME, not its line style. A bus name is NAME[high_index . .0], i.e., DIN[3..0]. You add this label to a net by clicking on the net and typing the text. To label individual nets that make up bits of the bus, use names like DIN0, DIN1, DIN2, etc. You do NOT have to physically connect the individual nets to the bus; the names on the nets are used to determine

what nets segments are actually connected (look in the REG4BIT schematic - I have the DIN bus physically connected to all of its individual nets, but the DOUT bus is not physically connected - it is only connected via its naming convention.

8. The menu symbol that looks like a little 'factory' is the compile command. You have to compile your schematic before simulation.
9. To use the REG1BIT schematic in the REG4BIT schematic, you will need to create a symbol for Reg1bit. Use the command File -> Create Default Symbol to create the symbol.

Tips on Simulation/WaveForm Editing

1. To create a new waveform window, use File -> New -> Waveform editor file
2. To insert a node (a waveform) , RIGHT CLICK and do Insert Node. If your waveform editor file is named the same as the graphic file, then you can use the 'List' button to list all available nodes and choose one.
3. To change the value of portion of the waveform, click and drag on the portion of the waveform to change - then click on either the '1' or '0' button along the left hand side to change this portion to a 1 or 0.
4. To set the END TIME of the simulation waveform, make sure the waveform window is selected, then use File -> End Time to set the ending time.
5. To insert a clock waveform, select the signal, RIGHT CLICK, and overwrite with a clock. The clock PERIOD is determined by the 2X the grid spacing -- use Options -> Grid Size to set the grid size. When using the OVERWRITE command to set the clock, you will be able to specify a multiplier to multiply the clock period by.
6. To change a value of bus, click and drag a portion of the waveform and click on the 'G' menu button on the left edge (change a group value). You will be able to type in a value for the bus.
7. To execute the simulator, do File -> Project -> Save & Simulator or click on the button with the waveform in the display. This will bring up a Simulator window. Use the 'Open SCF' button to bring your waveform window to the front. Then click on 'Start' to start the simulation.
8. Output signals like DOUT do not have to be edited by you. You must add these nodes to the waveform window, but their values will be updated when you run the simulator.

MaxPlus under Unix

To run maxplus under Unix do:

```
% swsetup altera
% max2win
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This will bring up the maxplus window. The first time this is done, a font cache will be built and this takes time. The next time you run *max2win*, it should not have to build this font cache.

You should probably create separate directories for each lab.