Virtex™ 2.5 V
Field Programmable Gate Arrays

November 9, 1998 (Version 1.1 - ADVANCE) Product Specification

Features

- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 50k to 1M system gates
  - System performance up to 200 MHz
  - 66-MHz PCI Compliant
  - Hot-swappable for Compact PCI
- Multi-standard SelectIO™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierachical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.22-µm five-layer metal process
- 100% factory tested

Description

The Virtex FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22-µm CMOS process. These advances make Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the nine members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Table 1: Virtex Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	BlockRAM Bits	Max Select RAM Bits
XCV50	57,906	16x24	1,728	180	32,768	24,576
XCV100	108,904	20x30	2,700	180	40,960	38,400
XCV150	164,674	24x36	3,888	260	49,152	55,296
XCV200	236,666	28x42	5,292	284	57,344	75,264
XCV300	322,970	32x48	6,912	316	65,536	98,304
XCV400	468,252	40x60	10,800	404	81,920	153,600
XCV600	661,111	48x72	15,552	500	98,304	221,184
XCV800	888,439	56x84	21,168	514	114,688	301,056
XCV1000	1,124,022	64x96	27,648	514	131,072	393,216

Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (SelectMAP™ and slave serial modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O.

Table 2: Performance for Common Circuit Functions

Function	Bits	Virtex -6
Register-to-Register		
Adder	16 64	5.0 ns 7.2 ns
Pipelined Multiplier	8 x 8 16 x 16	5.1 ns 6.0 ns
Address Decoder	16 64	4.4 ns 6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9 18 36	4.1 ns 5.0 ns 6.9 ns
Chip-to-Chip		
HSTL Class IV		200 MHz
LVTTL,16mA, fast slew		180 MHz

Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many designs operated internally at speeds in excess of 100 MHz and can achieve 200 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Architectural Description

Virtex Array

The Virtex user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

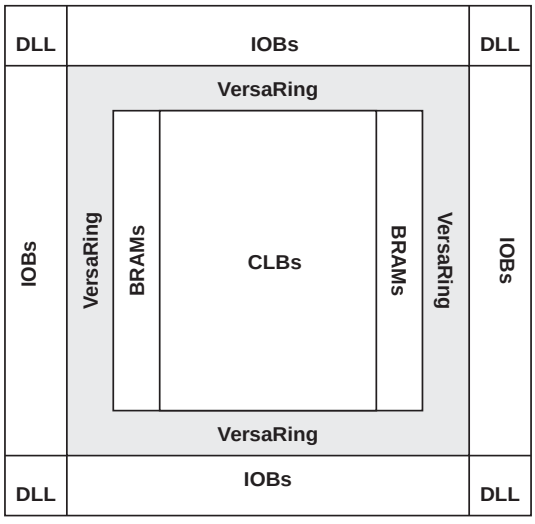

Figure 1: Virtex Architecture Overview

A set of Supplementary Description documents published separately augment the following description of the various Virtex-architecture components. The Supplementary Descriptions provide more detailed information and cover the following topics.

- Input/Output Block
- Configurable Logic Block
- Memory Resources
- Clock Distribution
- Routing Resources
- Configuration and Readback
- Boundary Scan
- Power Consumption

Input/Output Block

The Virtex IOB, Figure 2, features SelectIO™ inputs and outputs that support a wide variety of I/O signalling standards, see Table 3. These high-speed inputs and outputs are capable of supporting PCI interfaces up to 66 MHz.

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The input and output buffers and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5-V compliance, and one that does not. For 5-V compliance, a zener-like structure connected to ground turns on when the output rises to approximately 6.5 V. When 5-V compliance is not required, a conventional clamp diode may be connected to the output supply voltage, V_{CCO}. The type of over-voltage protection can be selected independently for each pad.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-up and pull-down resistors and the weak-keeper circuit are inactive, and input floats. If the design requires a defined input logic level prior to configuration, an external resistor must be used.

All Virtex IOBs support IEEE 1149.1-compatible boundary scan testing.

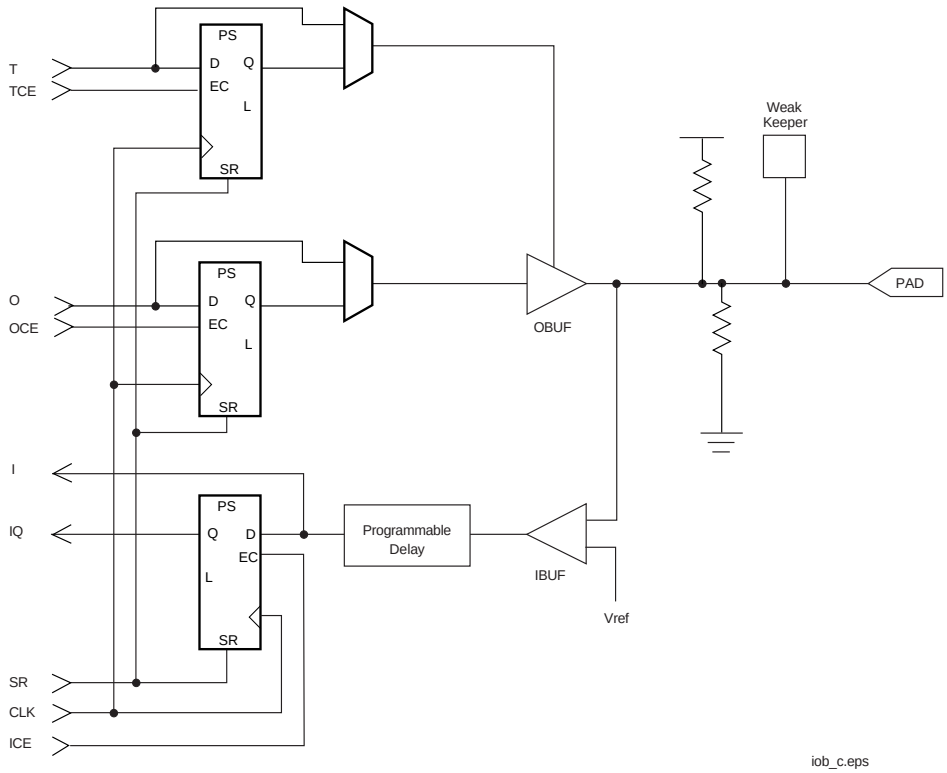

Figure 2: Virtex Input/Output Block (IOB)

Table 3: Supported Select I/O Standards

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL 2 – 24 mA	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	1.5
HSTL Class III	0.75	1.5	1.5
HSTL Class IV	0.75	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.125	2.5	1.125
CTT	1.5	3.3	1.5
AGP	1.32	3.3	N/A

Input Path

A buffer In the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See “I/O Banking” on page 4.

There are optional pull-up and pull-down resistors at each input for use after configuration. Their value is in the range 50 – 150 kohms.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 4.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

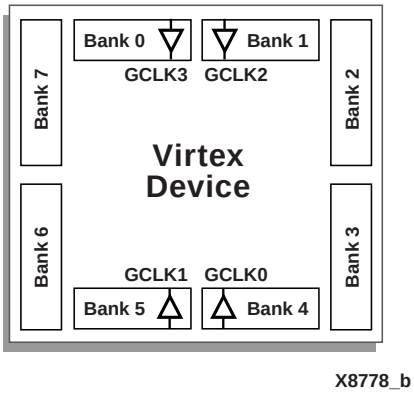

Figure 3: Virtex I/O Banks

Within a bank, output standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 4: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage may be used within a bank.Input buffers that use V_{REF} are not 5V-tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins may be left unconnected externally, or may be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

In HQ and PQ packages, all V_{CCO} pins are bonded together internally, and consequently the same V_{CCO} voltage must be connected to all of them. The V_{REF} pins remain internally connected as eight banks, and may be used as described previously.

Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous Set and Reset signals (SR and BY). Alternatively, these signals may be configured as asynchronous Preset and Clear

All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

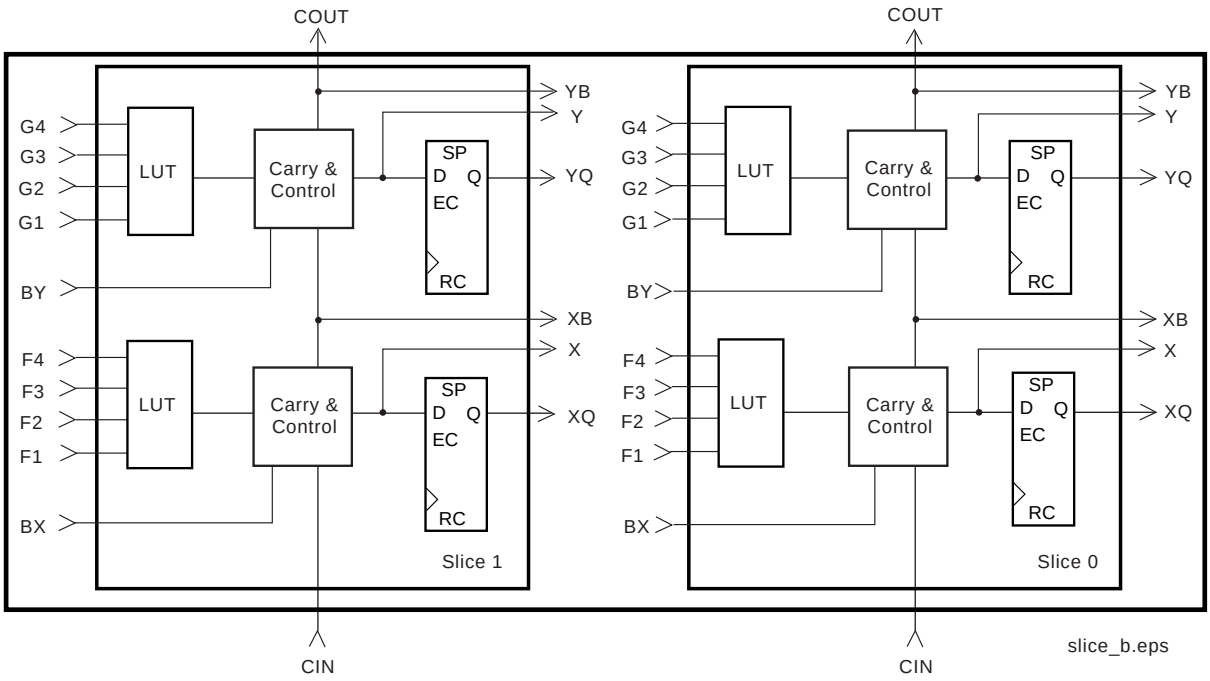

Figure 4: 2-slice Virtex CLB

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See “Dedicated Routing” on page 9. Each Virtex BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Virtex FPGAs incorporate several large BlockSelectRAM+ memories. These complement the distributed SelectRAM+ LUTRAMs that provide shallow RAM structures implemented in CLBs.

BlockSelectRAM+ memory blocks are organized in columns. All Virtex devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Virtex device 64 CLBs high will contain16 memory blocks per column, and a total of 32 blocks.

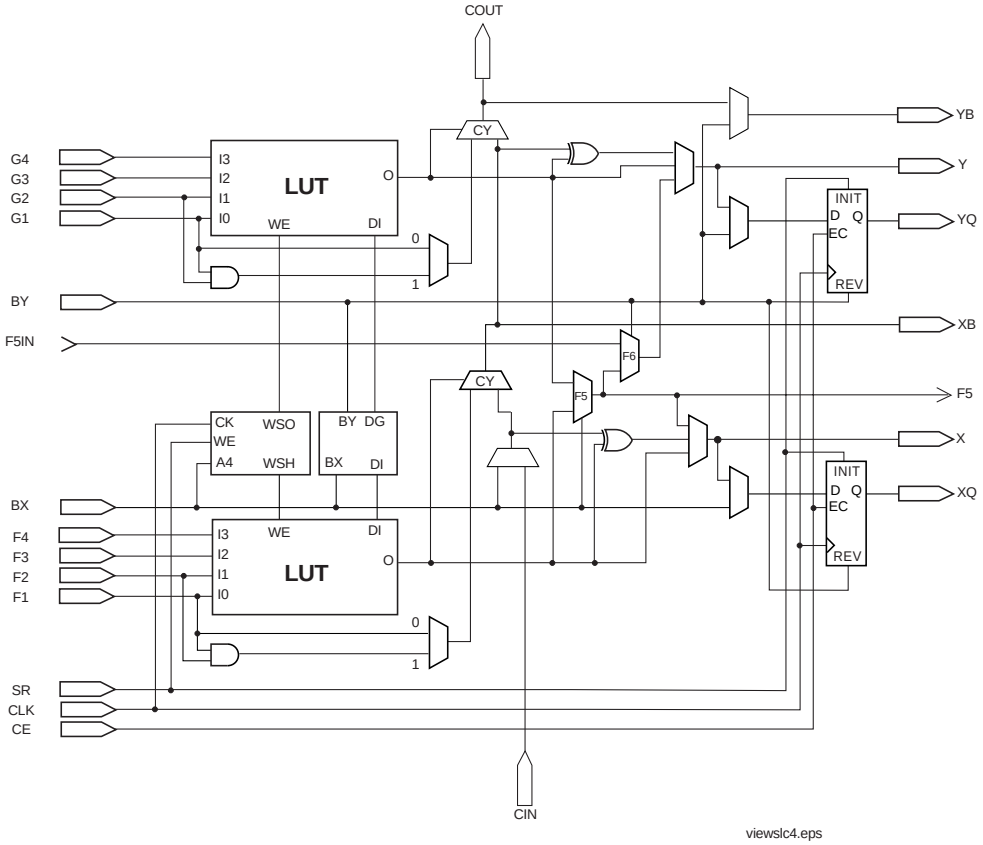

Figure 5: Detailed View of Virtex Slice

Table 5 shows the amount of Block SelectRAM+ memory that is available in each Virtex device.

Each Block SelectRAM+ cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 5: Virtex Block SelectRAM+ Amounts

Virtex Device	# of Blocks	Total Block SelectRAM+ Bits
XCV50	8	32,768
XCV100	10	40,960
XCV150	12	49,152
XCV200	14	57,344
XCV300	16	65,536
XCV400	20	81,920
XCV600	24	98,304
XCV800	28	114,688
XCV1000	32	131,072

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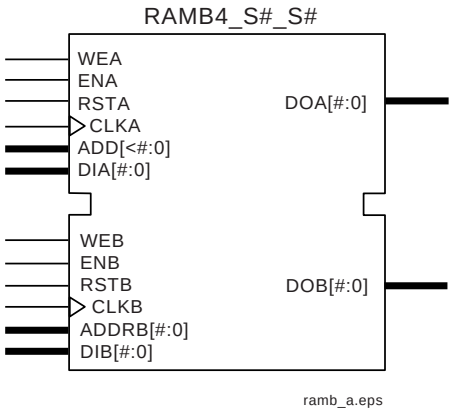

Figure 6: Dual-Port Block SelectRam+

Table 6 shows the depth and width aspect ratios for the Block SelectRAM+

Table 6: Block SelectRAM+ Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Virtex block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

General Purpose Routing

Most Virtex signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Virtex devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

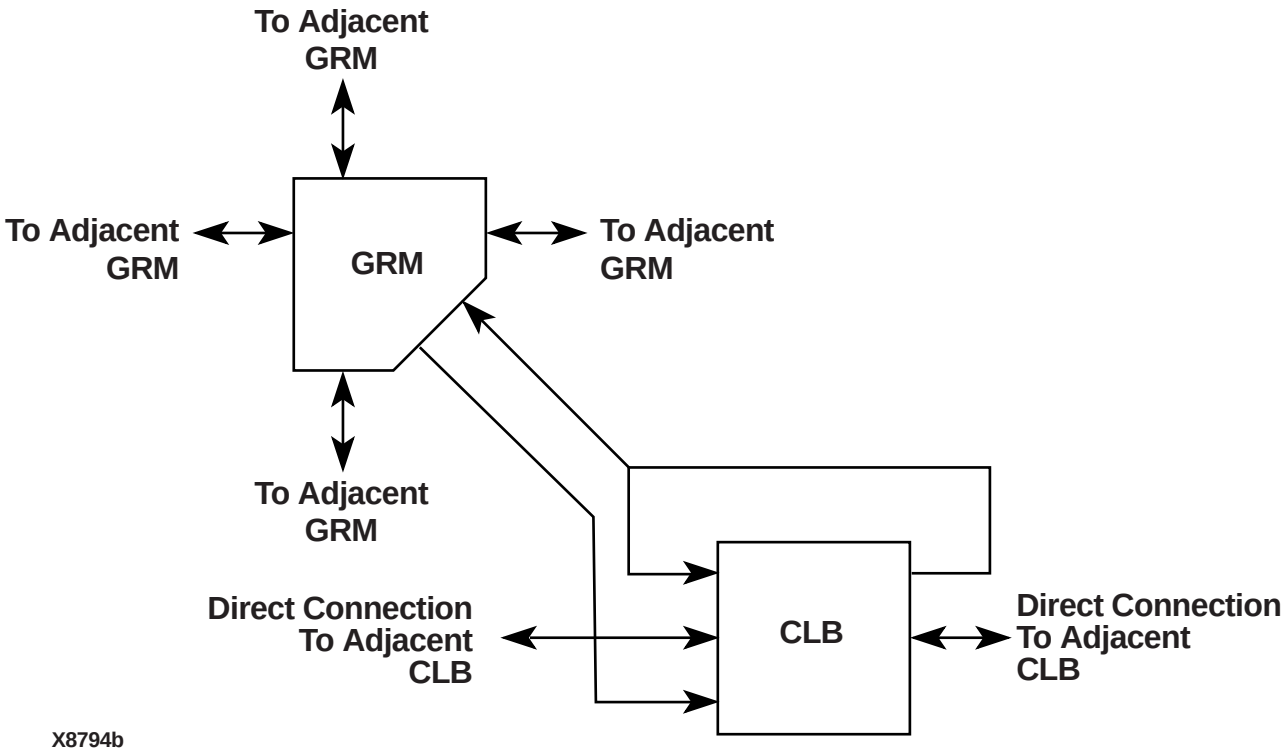

Figure 7: Virtex Local Routing

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only

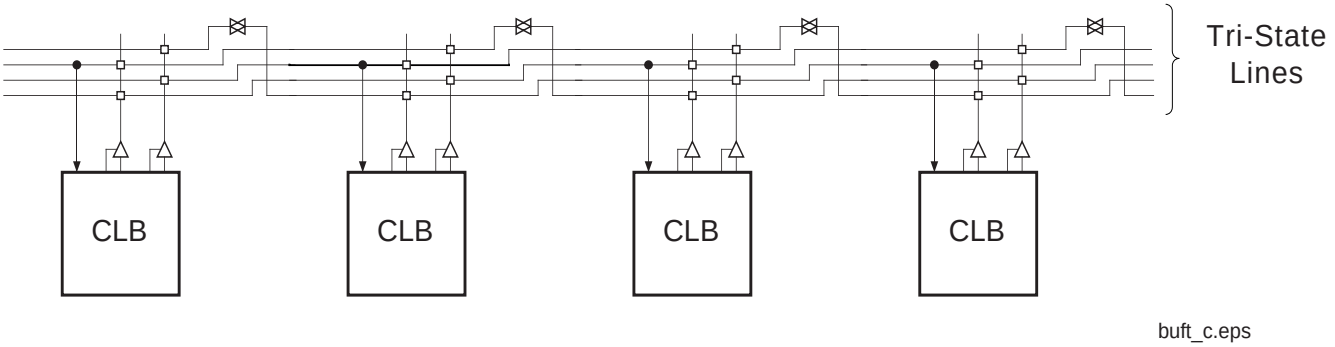

Figure 8: BUFT Connections to Dedicated Horizontal Bus Lines

be driven by global buffers. There are four global buffers, one for each global net.

- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

Virtex provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 9.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

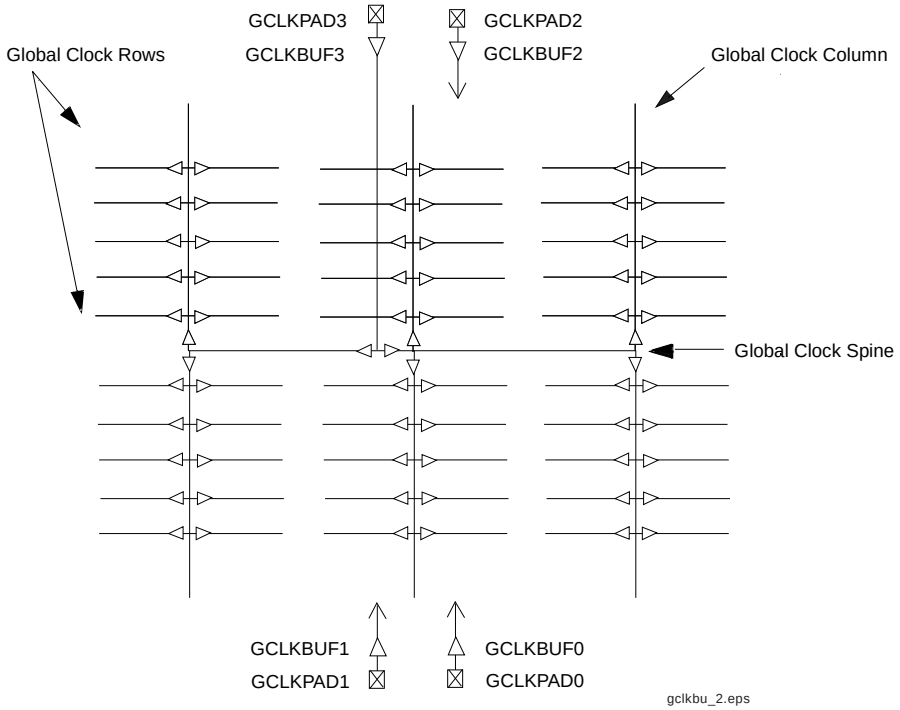

Figure 9: Global Clock Distribution Network

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins. This technique partially compensates for the absence of INTEST support.

Table 7: Boundary-Scan Instructions

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan intest operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Tri-states output pins while enabling the Bypass Register
BUS_RST	01011	Reset the Configuration Bus
JSTART	01100	Clock the startup sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Development System

Virtex FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Virtex design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others may be re-used as general purpose inputs and outputs once configuration is complete.

The dedicated pins are the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the PROGRAM pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the configuration mode chosen, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

For a more detailed description than that given below, see the Supplementary Description on Configuration and Readback.

Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select these configuration modes. The selection codes are listed in Table 8. Note that unlisted selection codes are reserved.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Table 8: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D_{out}
Master-serial mode	0	0	0	Out	1	Yes
Boundary-scan mode	1	0	1	N/A	1	No
SelectMAP mode	1	1	0	In	8	No
Slave-serial mode	1	1	1	In	1	Yes

Slave Serial Mode

In slave serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The capture of DIN on the rising edge of CCLK differs from previous families, but will not cause a problem for mixed configuration chains. This change was made to improve serial-configuration rates for Virtex only chains.

Figure 10 shows a full master/slave system. A Virtex device in slave serial mode should be connected as shown in the third device from the left

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. Figure 11 shows slave-serial configuration timing.

Table 9 provides more detail about the characteristics shown in Figure 11. Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

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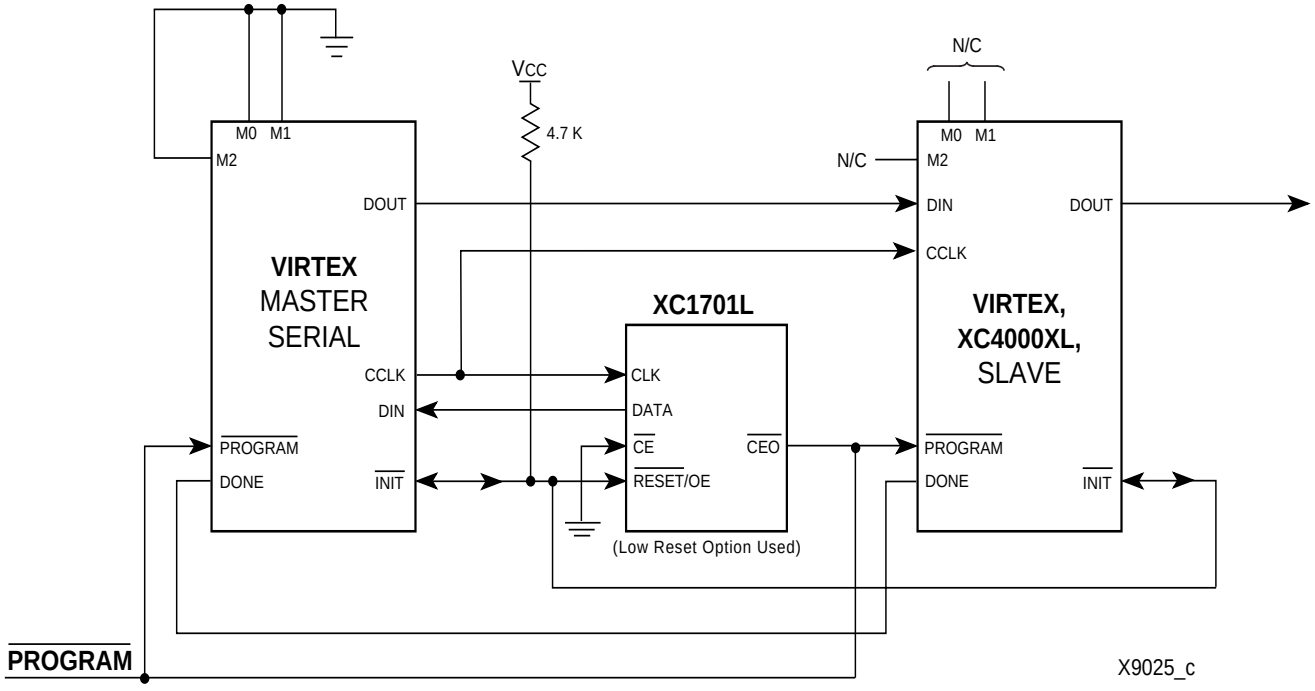

Figure 10: Master/Slave Serial Mode Circuit Diagram

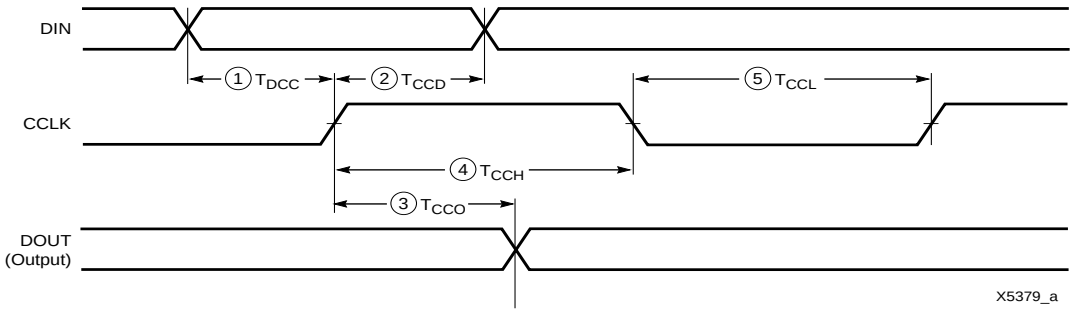

Figure 11: Slave Serial Mode Programming Switch

Table 9: Slave Serial Mode Programming Switching

	Description	Symbol			Units
CCLK	DIN setup/hold	1/2	T_{DCC}/T_{CCD}	2.0/0.0	ns, min
	DOUT	3	T_{CCO}	9.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max

Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The preamble is also forwarded to other devices in the daisy-chain.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support this rate.

Figure 10 shows a full master/slave system. In this system, the leftmost device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and CE input is driven by DONE. There is, therefore, the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 12.

Figure 13 shows the timing of master-serial configuration. Master serial mode is selected by a <000> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 13

At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until Vcc is valid.

Table 10: Master Serial Mode Programming Switching

	Description	Symbol			Units
CCLK	DIN setup/hold	1/2	T_{DSCK}/T_{SCKD}	2.0/0.0	ns, min

Note: Master serial mode timing is based on testing in slave mode.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-serial data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ($\overline{CS}$) signal and a Write signal ($\overline{WRITE}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If $\overline{WRITE}$ is not asserted, configuration data is read out of the FPGA as part of a readback operation.

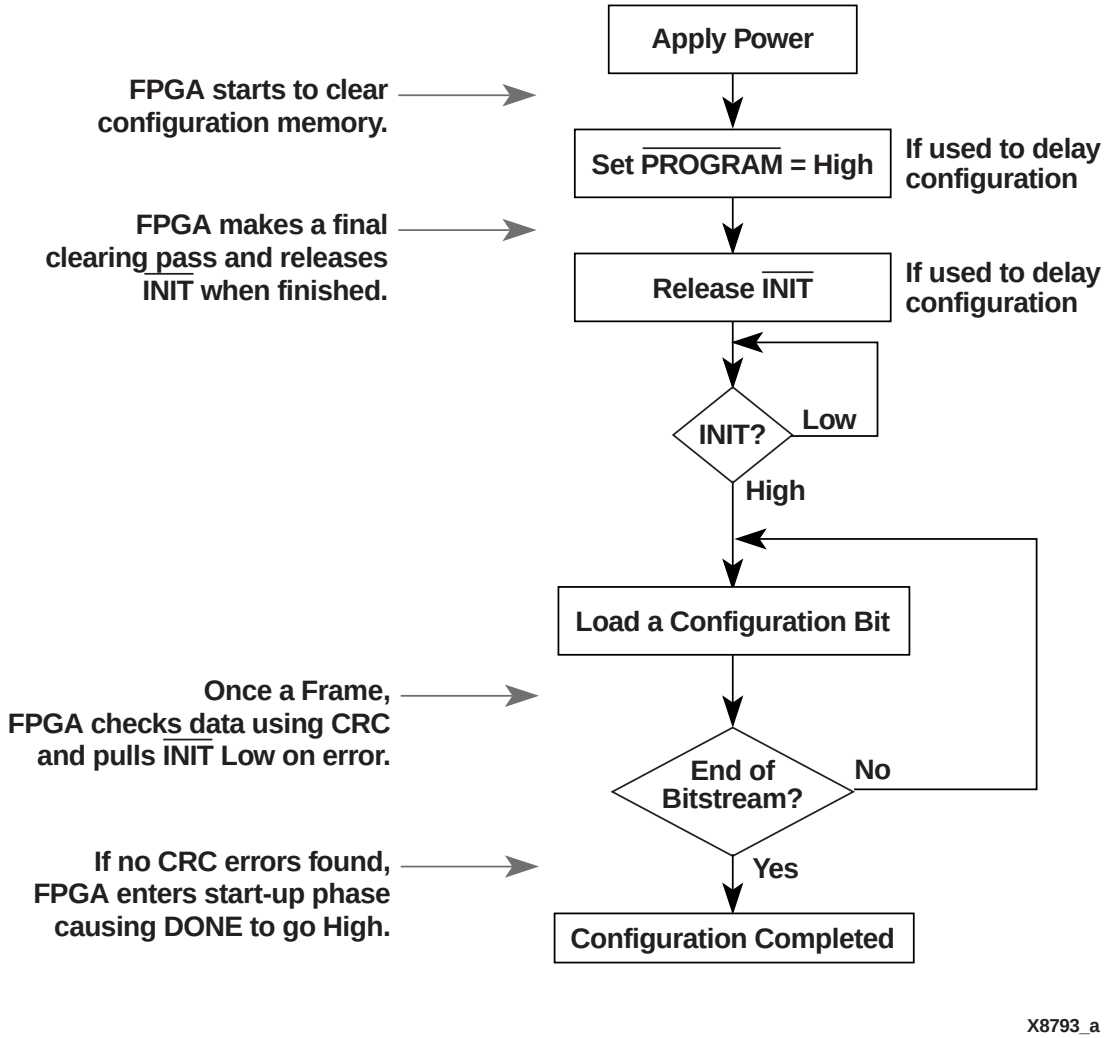

Figure 12: Serial Configuration Flowchart

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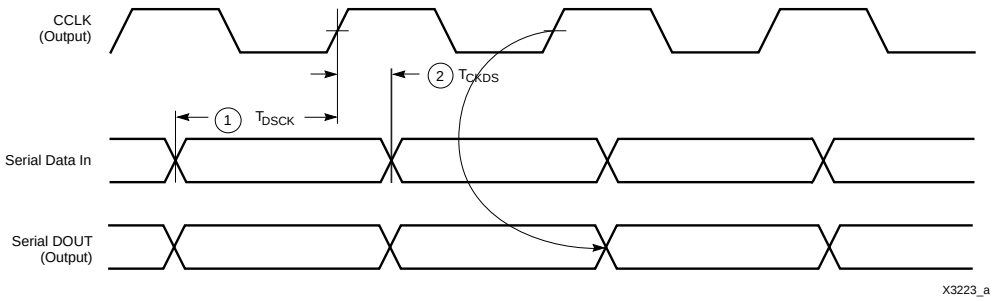

Figure 13: Master Serial Mode Programming Switching Characteristics

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data.

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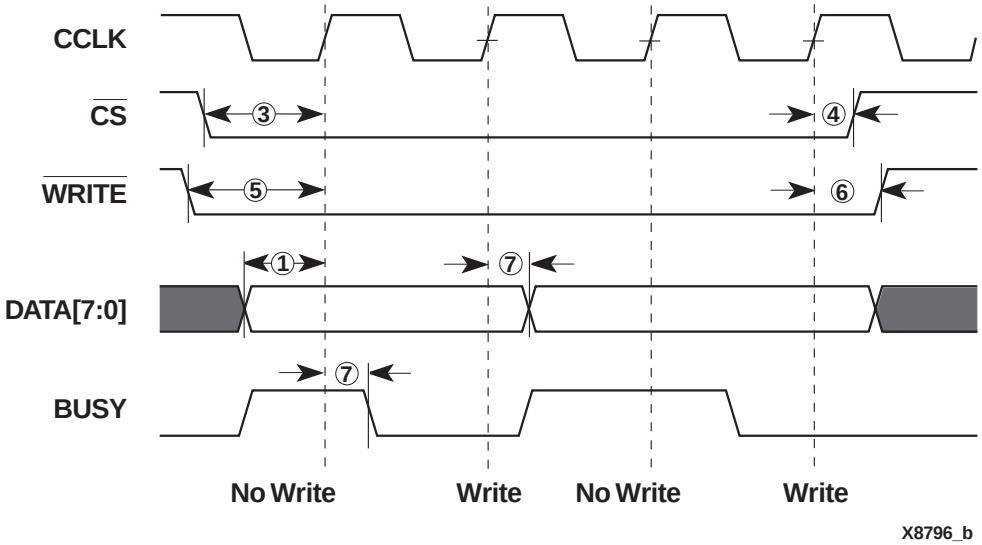


Figure 14: SelectMAP Write Waveforms

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 14.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or deasserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more that one CS should be asserted.
3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High from a previous write, the data is not be accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. Deassert CS and WRITE.

A flowchart for the write operation appears in Figure 15. Note that if CCLK is slower than f_{CCNH}, the FPGA will never assert BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Table 11: SelectMAP Write Timing Characteristics

	Description	Symbol			Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	2.0/0.0	ns, min
	$\overline{CS}$ Setup/Hold	34	T_{SMCSCC}/T_{SMCCCS}	2.0/0.0	ns, min
	$\overline{WRITE}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	2.0/0.0	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	9.0	ns, max
	Maximum Frequency with no handshake		f_{CCNH}	50	MHz, max

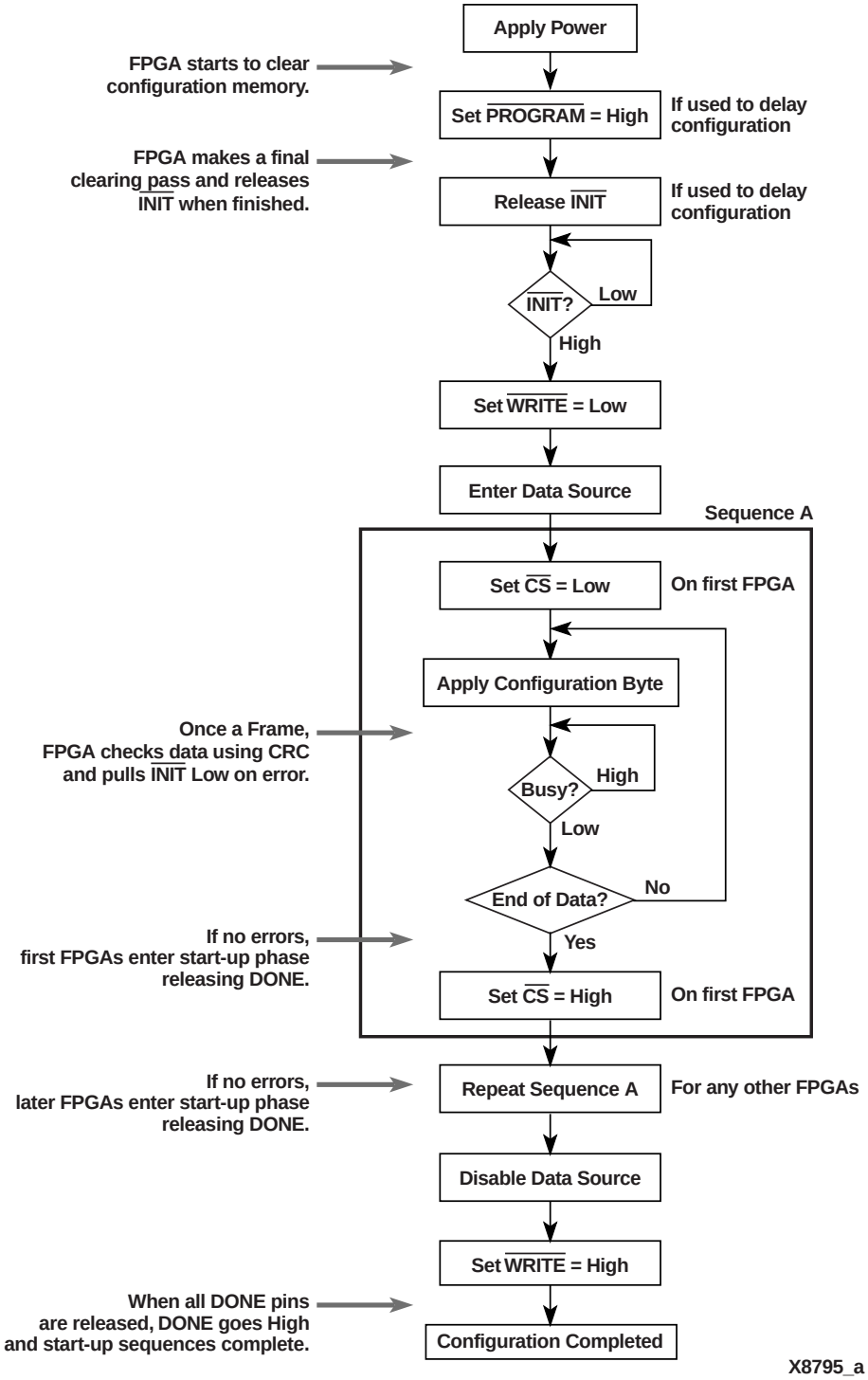


Figure 15: SelectMAP Flowchart for Write Operation

Abort

During a given assertion of CS, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, deassert WRITE. At the rising edge of CCLK, an abort is initiated, as shown in Figure 16.

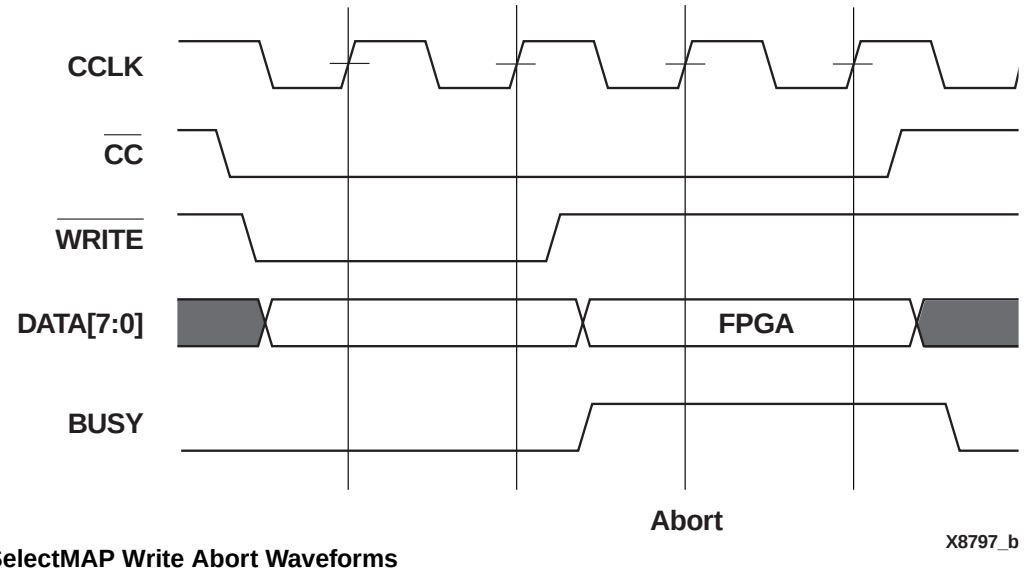


Figure 16: SelectMAP Write Abort Waveforms

Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK for the length of the sequence (the length is programmable)
8. Return to RTI

As noted above, configuration and readback is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <101> on the mode pins (M2, M1, M0).

Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process may also be initiated by asserting PROGRAM. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by asserting DONE.

Delaying Configuration

Configuration of the FPGA can be delayed by holding the PROGRAM pin Low until the system is ready for the device to configure. During the memory clearance phase, the configuration sequences continuously cycles through the configuration memory clearing all addresses. This activity continues until the completion of one full address cycle after the PROGRAM pin goes High. Thus, configuration is delayed by extending the memory clearance phase.

Alternatively, $\overline{INIT}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{INIT}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to act as if the configuration memory is still being cleared. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global tri-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events may be changed. In addition, the GTS, GSR, and GWE events may be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence may also be paused at any stage until lock has been achieved on any or all DLLs.

Data Stream Format

Virtex devices are configured by sequentially loading frames of data.that have been concatenated into a bitstream. Table 12 lists the total number of bits required to configure each device.

Table 12: Virtex Bit-stream Lengths

Device	# of Configuration Bits
XCV50	559,232
XCV100	781,248
XCV150	1,041,128
XCV200	1,335,872
XCV300	1,751,840
XCV400	2,546,080
XCV600	3,608,000
XCV800	4,715,584
XCV1000	6,127,772

Readback

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information contact the factory for a copy of the “Supplementary Description on Configuration and Readback”.

Pin Definitions

Table 13: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode are pins used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectRAM and slave-serial modes, and output in master-serial mode
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Output	Indicates that configuration loading is complete, and that the start-up sequence is in progress.
$\overline{\text{INIT}}$	No	Bidir (open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input	In SelectMAP mode, D0-7 are configuration data input pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
$\overline{\text{CS}}$	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, Cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Virtex DC Characteristics

Definition of Terms

Data sheets may be designated as Advance or Preliminary. The status of specifications in these data sheets is as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Data sheets not identified as either Advance or Preliminary are to be considered final.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex Absolute Maximum Ratings

Symbol	Description			Units
V_{CCINT}	Supply voltage relative to GND		-0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{REF}	Input Reference Voltage		-0.5 to 3.6	V
V_{IN}	Input voltage relative to GND, differential inputs		-0.5 to 3.6	V
V_{IN}	Input voltage relative to GND, other pins		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output		-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+125	°C
		Plastic packages	+125	°C

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Virtex Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.5 - 5%	2.5 + 5%	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	2.5 - 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial		3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial		3.6	V
T_{IN}	Input signal transition time			250	ns

Notes: Correct operation is guaranteed with a minimum V_{CCINT} of 2.25 V (Nominal V_{CCINT} -10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50-mV reduction in V_{CCINT} below the specified range.
At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

Virtex DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)		2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)		1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)				mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)				mA
I_{REF}	V_{REF} current per V_{REF} pin			20	µA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		Note 2	0.15	mA

Note 1: With no output current loads, no active input pull-up resistors, all I/O pins Tri-stated and floating.
Note 2: Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Virtex DC Input and Output levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL (Note 1)	0.0	0.8	2.0	5.5	0.4	2.4	24	- 24
LVCMOS2	0.0	44% V_{CCINT}	60% V_{CCINT}	5.5	10% V_{CCO}	90% V_{CCO}	1.5	- 0.5
PCI, 3.3 V	- 0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	- 0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	0.0	V_{REF} - 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a
HSTL I	0.0	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL III	0.0	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL IV	0.0	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
SSTL3 I	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.6	V_{REF} + 0.6	8	-8
SSTL3 II	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.8	V_{REF} + 0.8	16	-16
SSTL2 I	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.45	V_{REF} + 0.45	6	-6
SSTL2 II	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.6	V_{REF} + 0.6	12	-12
CTT	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
AGP	0.0	V_{REF} - 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Note1: V_{OL} and V_{OH} for lower drive currents are sample tested.
Note 2: Tested according to the relevant specifications.

Virtex Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

Virtex IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, these delays typically vary by less than 0.3 ns. Precise values are provided by the timing analyzer.

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Propagation Delays					
Pad to I output, no delay	T_{IOPI}	0.8	0.9	1.0	ns, max
Pad to I output, with delay	T_{IOPID}	1.4	1.6	1.8	ns, max
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	1.7	1.9	2.2	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	3.3	3.8	4.4	ns, max
Sequential Delays					
Clock CLK to output IQ	T_{IOCKIQ}	1.1	1.2	1.4	ns, max
Setup and Hold Times with respect to Clock CLK	Setup Time/Hold Time				
Pad, no delay	T_{IOPICK}/T_{IOICKP}	1.9/0.0	2.2/0.0	2.5/0.0	ns, min
Pad, with delay (Note 1)	$T_{IOPICKD}/T_{IOICKPD}$	3.5/<0	4.1/<0	4.7/<0	ns, min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	0.8/0.0	0.9/0.0	1.0/0.0	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}/T_{IOCKISR}$	0.8/0.0	1.0/0.0	1.1/0.0	ns, min
Set/Reset Delays					
SR input to IQ (asynchronous)	T_{IOSRIQ}	1.2	1.4	1.6	ns, max
GSR to output IQ	T_{GSRQ}				ns, max

Note 1: With delay, the IOB hold time is negative. This reduces or eliminates pad-to-pad hold time.

Virtex Pad-to-Pad Switching Characteristics

Output delays terminating at the pad are specified for LVTTL levels with 12 mA drive and slow slew rate (the default output standard). For other standards, these delays must be adjusted by adding the values shown in the Virtex IOB Output Switching Characteristics table.

			Speed Grade			
Description		**Symbol**	**-6**	**-5**	**-4**	**Units**
Using a DLL						
Pad-to-pad input data setup time before the clock						ns, min
Pad-to-pad input data hold time after the clock						ns, min
Pad-to-pad delay from clock input to data output						ns, max
Without a DLL						
Pad-to-pad input data setup time before the clock	All					ns, min
Pad-to-pad input data hold time after the clock	All					ns, min
Pad-to-pad delay from clock input to data output	XCV50					ns, max
	XCV100					ns, max
	XCV150					ns, max
	XCV200					ns, max
	XCV300					ns, max
	XCV400					ns, max
	XCV600					ns, max
	XCV800					ns, max
	XCV1000					ns, max

Virtex IOB Output Switching Characteristics

Output delays terminating at the pad are specified for LVTTL levels with 12 mA drive and slow slew rate (the default output standard). For other standards, these delays must be adjusted by adding the values shown.

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	4.1	5.3	6.1	ns, max
O input to Pad via transparent latch	T_{IOOLP}	4.3	5.5	6.4	ns, max
3-State Delays					
T input to Pad high-impedance	T_{IOTHZ}	1.1	1.3	1.5	ns, max
T input to valid data on Pad	T_{IOTON}	5.0	5.8	6.6	ns, max
T input to Pad high-impedance via transparent latch	$T_{IOTLPHZ}$	1.7	1.9	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	5.0	5.8	6.6	ns, max
GTS to Pad high impedance	T_{GTS}	5.0	5.8	6.7	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	5.8	6.7	7.7	ns, max
Clock CLK to Pad high-impedance (synchronous)	T_{IOCKHZ}	2.1	2.4	2.8	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	5.8	6.7	7.7	ns, max
Setup Times before Clock CLK					
O input	T_{IOOCK}	0.5	0.5	0.6	ns, min
OCE input	$T_{IOOCECK}$	0.8	0.9	1.0	ns, min
SR input (OFF)	$T_{IOSRCKO}$	0.8	1.0	1.1	ns, min
3-State SetupTimes					
TCE input	$T_{IOTCECK}$	0.8	0.9	1.0	ns, min
T input	T_{IOTCK}	0.2	0.2	0.3	ns, min
SR input (TFF)	$T_{IOSRCKT}$	0.8	1.0	1.1	ns, min
Hold Times after Clock CLK					
All Hold Times		0.0	0.0	0.0	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}	5.0	5.8	6.6	ns, max
SR input to Pad high-impedance (asynchronous)	T_{IOSRHZ}	2.3	2.6	3.0	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	6.0	6.8	7.9	ns, max
GSR to Pad	T_{GSRQ}				ns, max
Output Delay Adjustments					
Standard-specific increments for delays terminating at pads	LVTTL, Slow, 2 mA	13.3	15.2	17.5	ns
	4 mA	5.8	6.6	7.6	ns
	6 mA	3.0	3.5	4.0	ns
	8 mA	1.2	1.4	1.6	ns
	12 mA	0.0	0.0	0.0	ns
	16 mA	- 0.2	- 0.2	- 0.3	ns
	24 mA	- 0.6	- 0.7	- 0.8	ns
	LVTTL, Fast, 2 mA	11.5	13.3	15.3	ns
	4 mA	3.5	4.1	4.7	ns
	6 mA	1.3	1.5	1.7	ns
	8 mA	- 0.9	- 1.0	- 1.2	ns
	12 mA	- 1.9	- 2.2	- 2.5	ns
	16 mA	- 2.0	- 2.3	- 2.7	ns
	24 mA	- 2.3	- 2.6	- 3.0	ns
	LVCMOS2	- 2.0	- 2.3	- 2.7	ns
	PCI, 33 MHz, 3.3 V	0.3	0.4	0.4	ns
	PCI, 33 MHz, 5.0 V	- 0.9	- 1.1	- 1.2	ns
	PCI, 66 MHz, 3.3 V	- 2.7	- 3.1	- 3.6	ns
	GTL	- 2.6	- 3.0	- 3.5	ns
	GTL+	- 1.9	- 2.2	- 2.5	ns
	HSTL I	- 2.8	- 3.2	- 3.7	ns
	HSTL III	- 2.8	- 3.3	- 3.7	ns
	HSTL IV	- 3.0	- 3.4	- 3.9	ns
	SSTL3 I	- 2.5	- 2.8	- 3.3	ns
	SSTL3 II	- 3.0	- 3.4	- 3.9	ns
	SSTL2 I	- 2.4	- 2.7	- 3.2	ns
	SSTL2 II	- 2.8	- 3.2	- 3.7	ns
	CTT	- 2.5	- 2.9	- 3.4	ns
	AGP	- 2.8	- 3.3	- 3.8	ns

Virtex CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	1.0	1.1	1.2	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	1.0	1.2	1.3	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	1.2	1.4	1.6	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.4	0.5	0.6	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.4	0.5	0.6	ns, max
BY input to YB output	T_{BYYB}	0.5	0.6	0.7	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	1.1	1.3	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.7	0.7	0.9	ns, max
Setup Times before Clock CLK					
4-input function: F/G Inputs	T_{ICK}	1.0	1.1	1.2	ns, min
5-input function: F/G inputs	T_{IF5CK}	1.4	1.6	1.8	ns, min
6-input function: F5IN input	T_{F5INCK}	0.8	0.9	1.0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}	1.6	1.8	2.0	ns, min
BX/BY inputs	T_{DICK}	1.6	1.8	2.0	ns, min
CE input	T_{CECK}	0.8	0.9	1.0	ns, min
SR/BY inputs (synchronous)	T_{RCK}	1.3	1.5	1.7	ns, min
Hold Times after Clock CLK					
All Hold Times		0.0	0.0	0.0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	2.0	2.3	2.6	ns, min
Minimum Pulse Width, Low	T_{CL}	2.0	2.3	2.6	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}	2.9	3.4	3.9	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.6	1.9	2.2	ns, max
Delay from GSR to XQ/YQ outputs	T_{GSRQ}				ns, max

Virtex CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Combinatorial Delays					
F operand inputs to X via XOR	T_{OPX}	0.8	0.9	1.0	ns, max
F operand input to XB output	T_{OPXB}	1.2	1.4	1.6	ns, max
F operand input to Y via XOR	T_{OPY}	1.6	1.9	2.2	ns, max
F operand input to YB output	T_{OPYB}	1.3	1.5	1.7	ns, max
F operand input to COUT output	T_{OPCYF}	1.3	1.5	1.7	ns, max
G operand inputs to Y via XOR	T_{OPGY}	1.0	1.1	1.3	ns, max
G operand input to YB output	T_{OPGYB}	1.4	1.6	1.9	ns, max
G operand input to COUT output	T_{OPCYG}	1.4	1.6	1.8	ns, max
BX initialization input to COUT	T_{BXCY}	0.8	0.9	1.0	ns, max
CIN input to X output via XOR	T_{CINX}	0.5	0.5	0.6	ns, max
CIN input to XB	T_{CINXB}	0.1	0.1	0.1	ns, max
CIN input to Y via XOR	T_{CINY}	0.5	0.6	0.7	ns, max
CIN input to YB	T_{CINYB}	0.2	0.2	0.2	ns, max
CIN input to COUT output	T_{BYP}	0.1	0.2	0.2	ns, max
Multiplier Operation					
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.4	0.5	0.6	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.5	0.6	0.6	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.5	0.5	0.6	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.4	0.4	0.5	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.4	0.4	0.5	ns, max
Setup Times before Clock CLK					
CIN input to FFX	T_{CCKX}	0.8	0.9	1.1	ns, min
CIN input to FFY	T_{CCKY}	0.9	1.0	1.1	ns, min
Setup Time Adjustment					ns
Hold Times after Clock CLK					
All Hold Times		0.0	0.0	0.0	ns, min

Virtex CLB SelectRAM Switching Characteristics

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Sequential Delays					
Clock CLK to X/Y outputs (WE active)					ns, max
Shift-Register Mode					
Clock CLK to X/Y outputs	T_{SHCKO}				ns, max
Setup Times before Clock CLK					
F/G address inputs	T_{AS}/T_{AH}	0.6	0.7	0.8	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	1.0	1.2	1.3	ns, min
CE input (WE)	T_{WS}/T_{WH}	0.6	0.6	0.7	ns, min
Shift-Register Mode					
BX/BY data inputs (DIN)	T_{SHDICK}				ns, min
CE input (WS)	T_{SHCECK}				ns, min
Hold Times after Clock CLK					
All Hold Times		0.0	0.0	0.0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	2.9	3.4	3.9	ns, min
Minimum Pulse Width, Low	T_{WPL}	2.9	3.4	3.9	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	5.8	6.7	7.7	ns, min

Virtex BLOCKRAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	3.3	3.8	4.4	ns, max
Setup Times before Clock CLK					
ADDR inputs	T_{BACK}	1.2	1.4	1.6	ns, min
DIN inputs	T_{BDCK}	1.2	1.4	1.6	ns, min
EN input	T_{BECK}	2.7	3.1	3.6	ns, min
RST input	T_{BRCK}	2.5	2.9	3.3	ns, min
WEN input	T_{BWCK}	2.4	2.8	3.2	ns, min
Hold Times after Clock CLK					
All Hold Times		0.0	0.0	0.0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}	2.0	2.3	2.6	ns, min
Minimum Pulse Width, Low	T_{BPWL}	2.0	2.3	2.6	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}				ns, min

Virtex TBUF Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.2	0.2	0.2	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.2	0.2	0.2	ns, max
Tri input to valid data on OUT output	T_{ON}	0.2	0.2	0.2	ns, max

Virtex Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
GCLK IOB and Buffer					
Global Clock PAD to output.	T_{GPID}	1.0	1.1	1.3	ns, max
IN input to OUT output	T_{GIO}	0.9	1.0	1.2	ns, max

Virtex Clock Distribution Guidelines

Description		Symbol	Speed Grade			Units
			-6	-5	-4	
GCLK Distribution						
From GCLK pad to any flip-flop	XCV50					ns, max
	XCV100					ns, max
Note: These clock-distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.	XCV150					ns, max
	XCV200					ns, max
	XCV300					ns, max
	XCV400					ns, max
	XCV600					ns, max
	XCV800					ns, max
	XCV1000					ns, max

Virtex Test Access Port Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
TMS and TDI Setup times before TCK					ns, min
TMS and TDI Hold times after TCK					ns, min
Output delay from clock TCK to output TDO					ns, max
Maximum TCK clock frequency					MHz, max

Virtex Pin Outs

Pin-Out Tables

Contact the factory for full pin-out listings of Virtex devices. For convenience, Table 14 and Table 15 list the locations of special-purpose and power-supply pins. Pins not listed are user I/Os.

Table 14: Virtex Pin-out Tables (Non-BGA)

Pin Name	Device	PQ/HQ240
GCK0	All	92
GCK1	All	89
GCK2	All	210
GCK3	All	213
M0	All	60
M1	All	58
M2	All	62
CCLK	All	179
$\overline{\text{PROGRAM}}$	All	122
DONE	All	120
$\overline{\text{INIT}}$	All	123
BUSY/DOUT	All	178
D0/DIN	All	177
D1	All	167
D2	All	163
D3	All	156
D4	All	145
D5	All	138
D6	All	134
D7	All	124
$\overline{\text{WRITE}}$	All	185
$\overline{\text{CS}}$	All	184
TDI	All	183
TDO	All	181

Table 14: Virtex Pin-out Tables (Non-BGA) (Continued)

Pin Name	Device	PQ/HQ240
TMS	All	2
TCK	All	239
V_{CCINT}	All	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225
V_{CCO}	All	15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
V_{REF}, Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	218, 232
	XCV100/150	... + 229
	XCV200/300	... + 236
	XCV400	... + 215
	XCV600	... + 230
	XCV800	... + 222
V_{REF}, Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	191, 205
	XCV100/150	... + 194
	XCV200/300	... + 187
	XCV400	... + 208
	XCV600	... + 193
	XCV800	... + 201
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	157, 171
	XCV100/150	... + 168
	XCV200/300	... + 175
	XCV400	... + 154
	XCV600	... + 169
	XCV800	... + 161

Table 14: Virtex Pin-out Tables (Non-BGA) (Continued)

Pin Name	Device	PQ/HQ240
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	130, 144
	XCV100/150	... + 133
	XCV200/300	... + 126
	XCV400	... + 147
	XCV600	... + 132
	XCV800	... + 140
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	97, 111
	XCV100/150	... + 108
	XCV200/300	... + 115
	XCV400	... + 94
	XCV600	... + 109
	XCV800	... + 101
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	70, 84
	XCV100/150	... + 73
	XCV200/300	... + 66
	XCV400	... + 87
	XCV600	... + 72
	XCV800	... +80
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	36, 50
	XCV100/150	... + 47
	XCV200/300	... + 54
	XCV400	... + 33
	XCV600	... + 48
	XCV800	... + 40

Table 14: Virtex Pin-out Tables (Non-BGA) (Continued)

Pin Name	Device	PQ/HQ240
V_{REF}, Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	9, 23
	XCV100/150	... + 12
	XCV200/300	... + 5
	XCV400	... + 26
	XCV600	... + 11
	XCV800	... + 19
GND	All	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233

Table 15: Virtex Pin-out Tables (BGA)

Pin Name	Device	BG256	BG352	BG432	BG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
$\overline{\text{PROGRAM}}$	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
$\overline{\text{INIT}}$	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
$\overline{\text{WRITE}}$	All	A19	D5	B4	D6
$\overline{\text{CS}}$	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

Table 15: Virtex Pin-out Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{CCINT} (V_{CCINT} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50/100/150/200	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19		
	XCV300		... + B16, D12, L1, L25, R23, T1, AF11, AF16	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22	
	XCV400/600			... + B26, C7, F1, F30, AE29, AF1, AH8, AH24	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25
	XCV800/1000				... + B12, C22, M3, N29, AB2, AB32, AJ13, AL22,
V_{CCO}, Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V_{CCO}, Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V_{CCO}, Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2

Table 15: Virtex Pin-out Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{CCO}, Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32
V_{CCO}, Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33
V_{REF}, Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	A8, B4			
	XCV100/150	... + A4	A16,C19, C21		
	XCV200/300		... + D21	B19, D22, D24, D26	
	XCV400		... + B15	... + C18	A19, D20, D26, E23, E27
	XCV600			... + C24	... + E24
	XCV800			... + B21	... + E21
	XCV1000				... + D29

Table 15: Virtex Pin-out Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF}, Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	A17, B12			
	XCV100/150	... + B15	B6, C9, C12		
	XCV200/300		... + D6	A13, B7, C6, C10	
	XCV400		... + C13	... + B15	A6, D7, D11, D16, E15
	XCV600			... + D10	... + D10
	XCV800			... + B12	... + D13
	XCV1000				... + E7
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	C20, J18			
	XCV100/150	... + F19	E2, H2, M4		
	XCV200/300		... + D2	E2, G3, J2, N1	
	XCV400		... + M1	... + R3	G5, H4, L5, P4, R1
	XCV600			... + H1	... + K5
	XCV800			... + M3	... + N5
	XCV1000				... + B3
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	M18, V20			
	XCV100/150	... + R19	R4, V4, Y3		
	XCV200/300		... + AC2	V2, AB4, AD4, AF3	
	XCV400		. + R1	... + U2	V4, W5, AD3, AE5, AK2
	XCV600			... + AC3	... + AF1
	XCV800			... + Y3	... + AA4
	XCV1000				... + AH4

Table 15: Virtex Pin-out Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	V12, Y18			
	XCV100/150	... + W15	AC12, AE5, AE8,		
	XCV200/300		... + AE4	AJ7, AL4, AL8, AL13	
	XCV400		... + AF12	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600			... + AK8	... + AL9
	XCV800			... + AJ12	... + AK13
	XCV1000				... + AN3
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	V9, Y3			
	XCV100/150	... + W6	AC15, AC18, AD20		
	XCV200/300		... + AE23	AJ18, AJ25, AK23, AK27	
	XCV400		... + AF15	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600			... + AL24	... + AM26
	XCV800			... + AH19	... + AN23
	XCV1000				... + AK28
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	M2, R3			
	XCV100/150	...+ T1	R24, Y26, AA25,		
	XCV200/300		... + AD26	V28, AB28, AE30, AF28	
	XCV400		... + P24	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600			... + AC28	... + AE31
	XCV800			... + Y30	... + AA30
	XCV1000				... + AH30

Table 15: Virtex Pin-out Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF}, Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	G3, H1			
	XCV100/150	... + D1	D26, G26, L26		
	XCV200/300		... + E24	F28, F31, J30, N30	
	XCV400		... + M25	... + R31	E31, G31, K31, P31, T31
	XCV600			... + J28	... + H32
	XCV800			... + M28	... + L33
	XCV1000				... + D31
GND	All	C3, C18, D4, D5, D9, D10, D11, D12, D16, D17. E4, E17, J4, J9, J10, J11, J12, J17, K4, K9, K10, K11, K12, K17, L4, L9, L10, L11, L12, L17, M4, M9, M10, M11, M12, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26	A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9 AL14, AL18 AL23, AL25, AL29, AL30	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
No Connect					C31, AC2, AK4, AL3

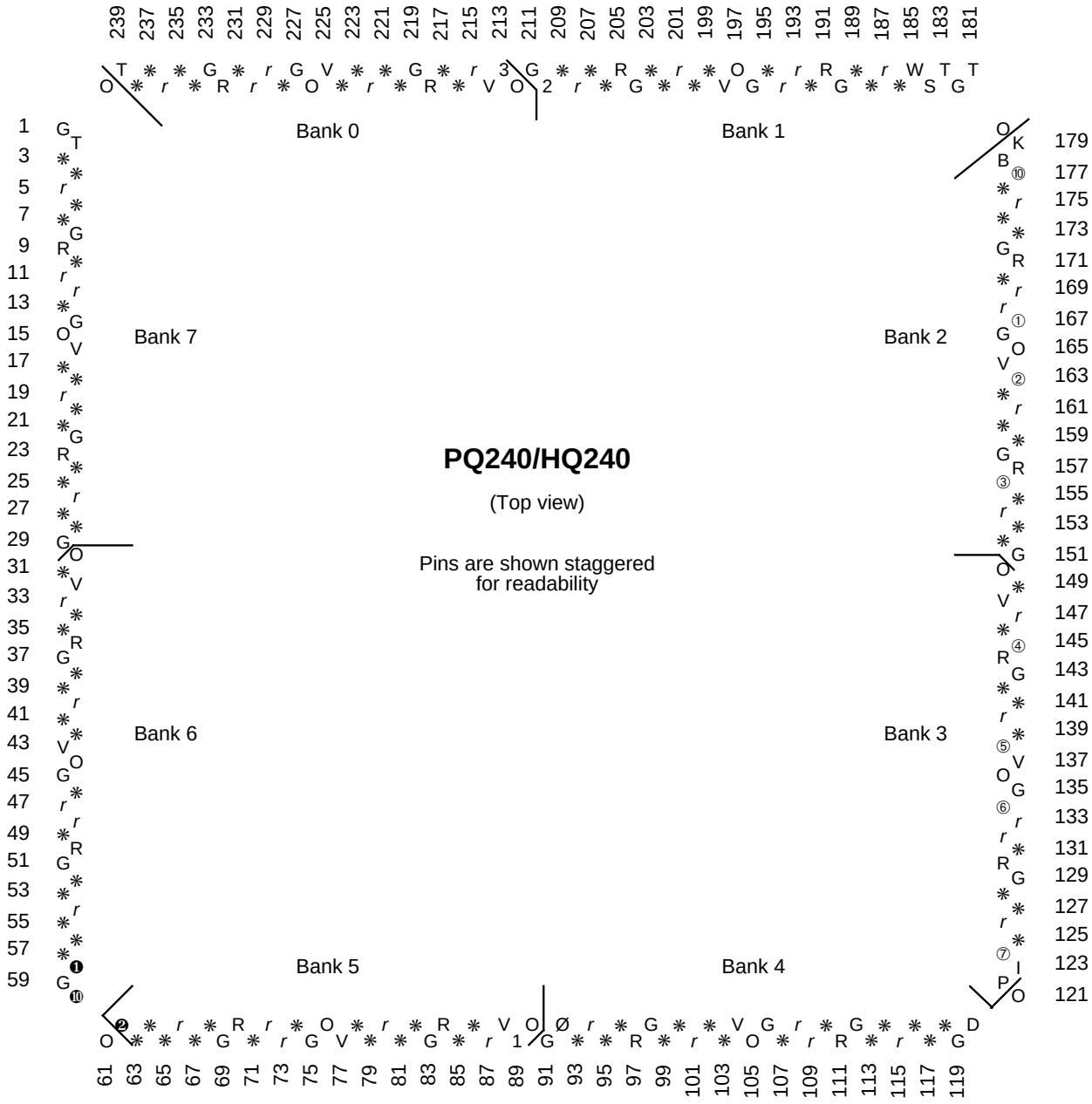
Pin-Out Diagrams

The following diagrams, pages 37 through 41, illustrate the locations of special-purpose pins on Virtex FPGAs. Table 16 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

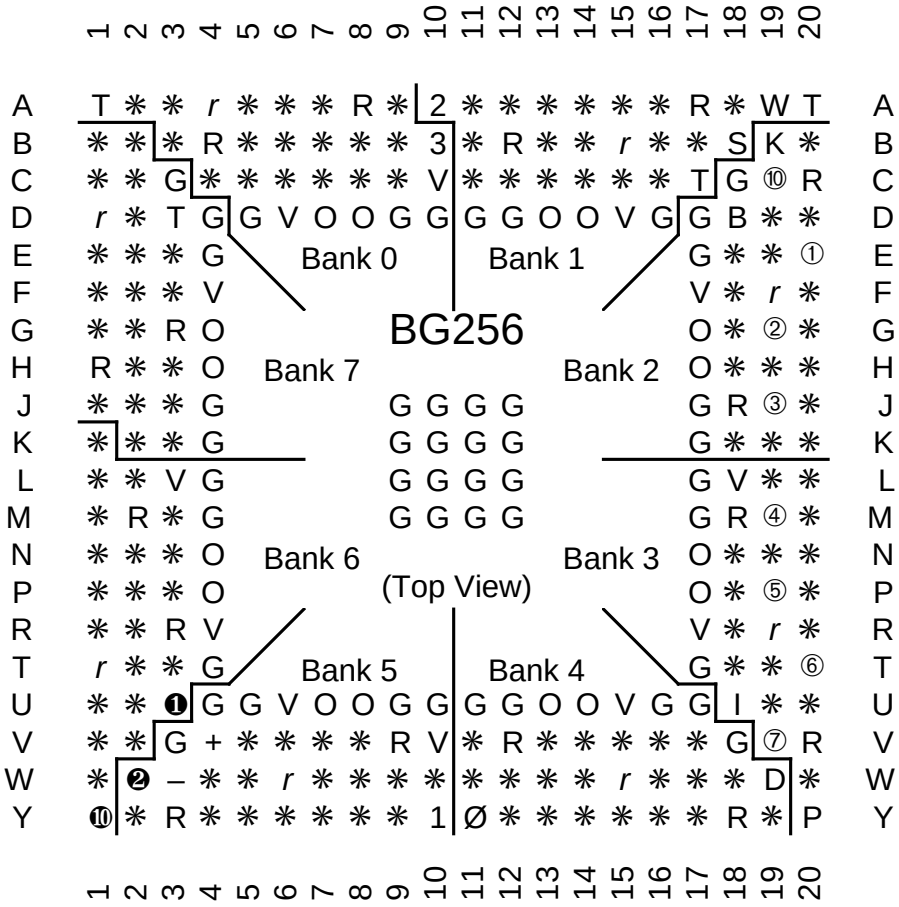
Table 16: Pin-out Diagram Symbols

Symbol	Pin Function
✳	General I/O
V	V_{CCINT}
v	Device-dependent V_{CCINT}, n/c on smaller devices
O	V_{CCO}
R	V_{REF}
r	Device-dependent V_{REF}, remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks
⓿, ❶, ❷	M0, M1, M2
⑩, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	$\overline{\text{PROGRAM}}$
I	$\overline{\text{INIT}}$
K	CCLK
W	$\overline{\text{WRITE}}$
S	$\overline{\text{CS}}$
T	Boundary-scan Test Access Port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

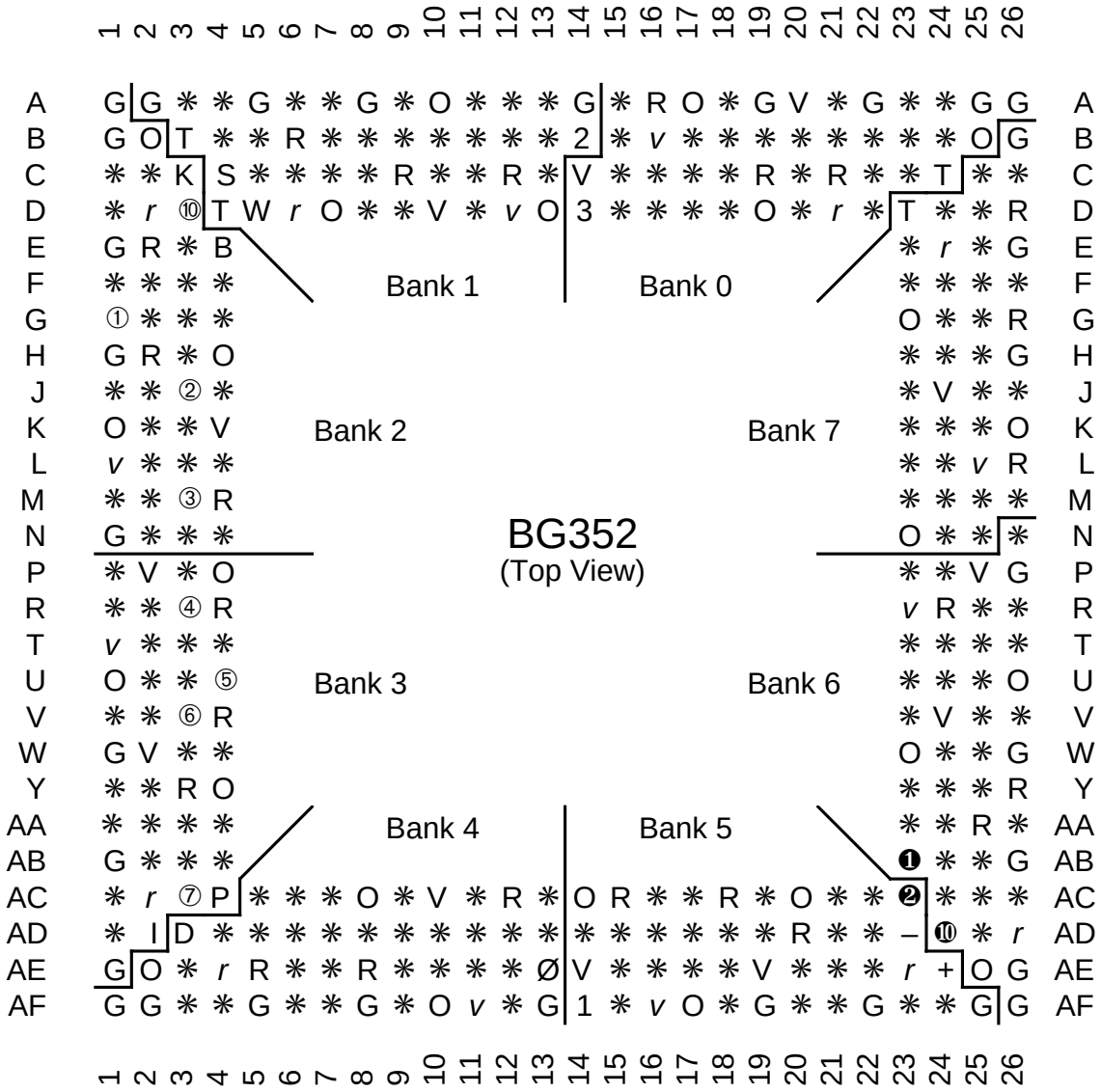
PQ240/HQ240 Pin-out Diagram



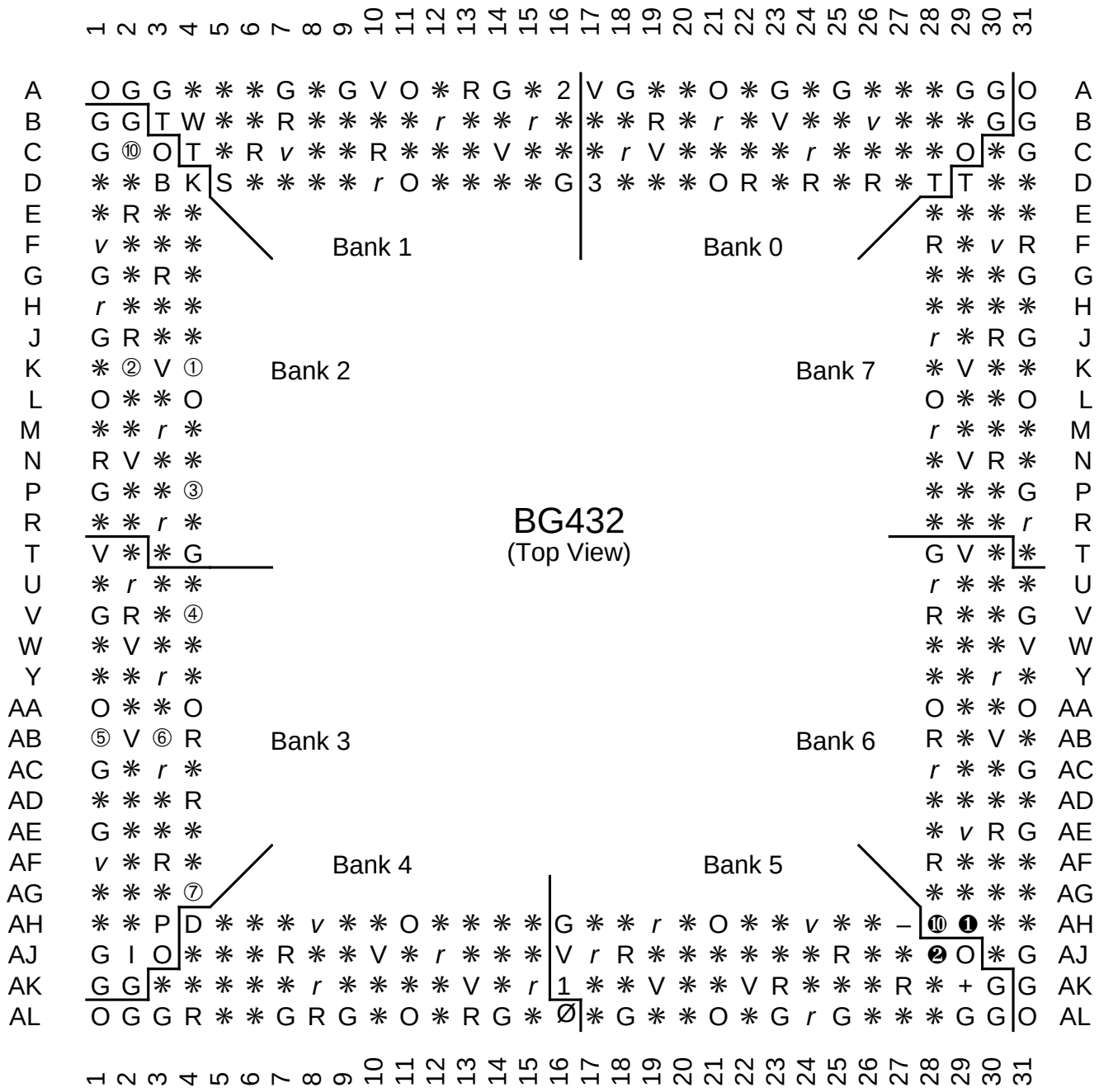
BG256 Pin-out Diagram



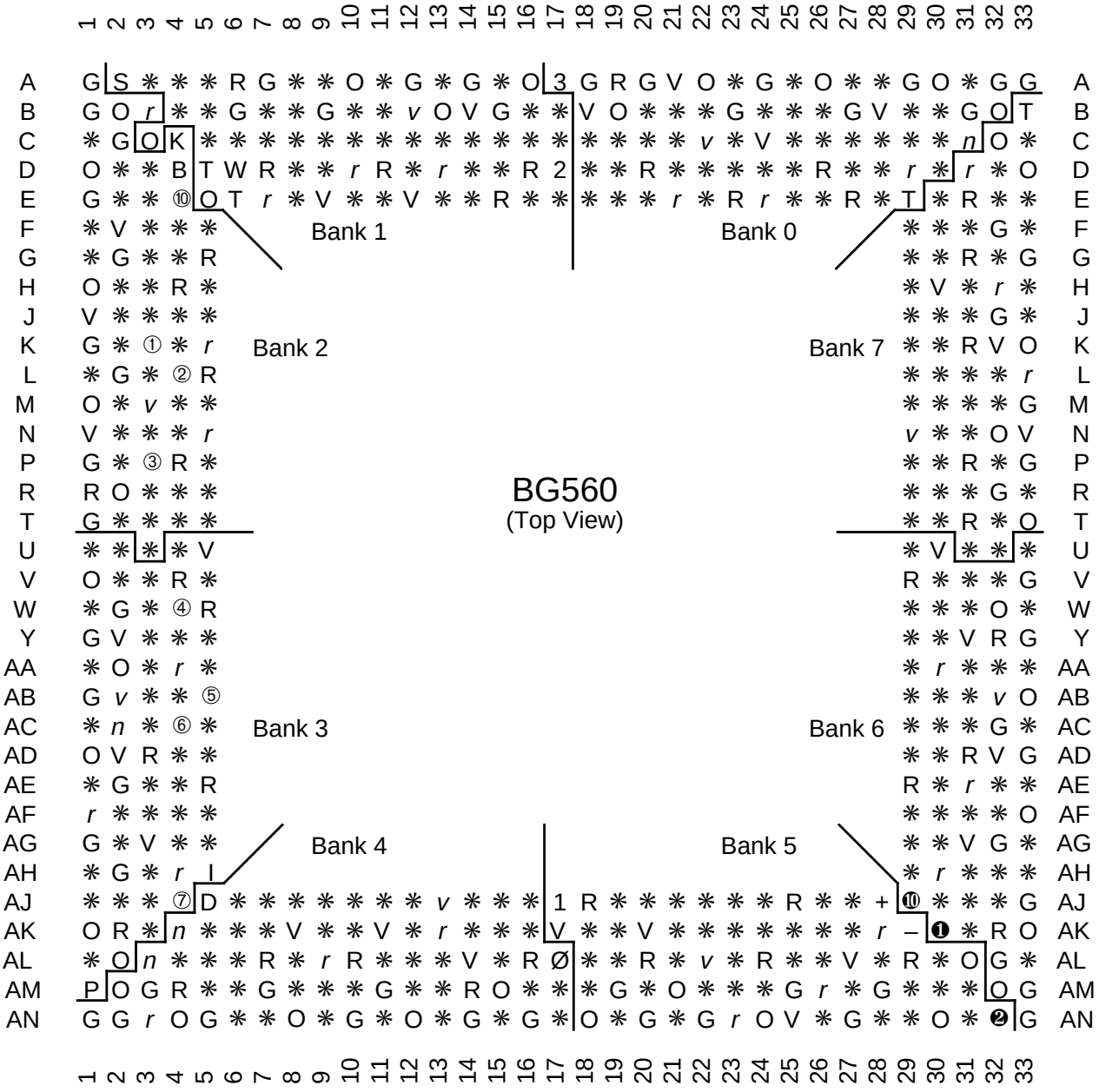
BG352 Pin-out Diagram



BG432 Pin-out Diagram



BG560 Pin-out Diagram



Device/Package Combinations and Maximum I/O

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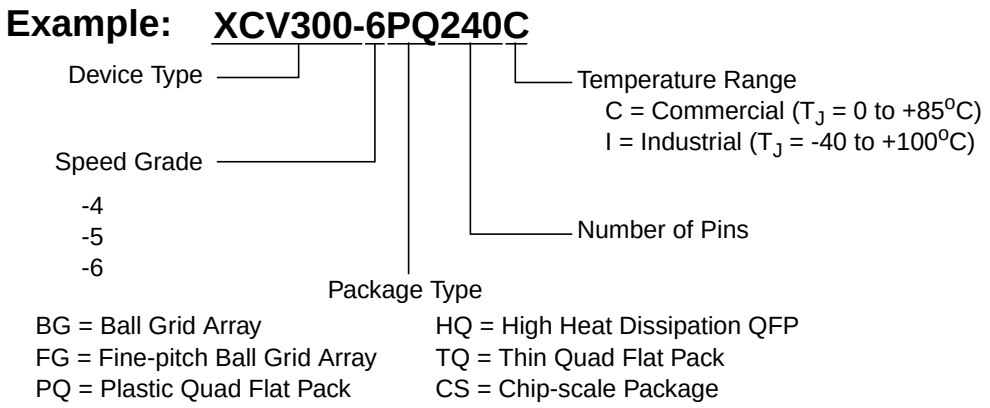
Package	Maximum User I/O								
	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	94	94							
PQ240	164	164	164	164	164				
HQ240						164	164	164	
BG256	180	180							
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG600						404	404	404	
FG680							500	514	514

Ordering Information



Revision Table

Date	Revision
11/98	Initial document release.