Three-Stating Actel Device I/O Pins for Board Level Testing

Introduction

During board testing and debugging, it is frequently desired or necessary to place all device I/O pins into a three-state, high-impedance condition. This isolates the device from other devices that have common signal paths on a printed circuit board. The three-state condition also allows board testing for trace integrity or insertion damage to pins. It is usually more convenient to simultaneously three-state all I/O pins of a device with a built-in procedure rather than to create test vectors to force this condition by circuit function.

All Actel field programmable gate arrays (FPGAs) include a special operating mode to place all I/O pins in a temporary, three-state condition. Thus, each Actel device may be easily isolated from I/O signal paths of other devices on a circuit board, enabling a convenient board testing procedure. This capability, combined with Silicon Explorer diagnostic tools, allows both single device and system board testing with a power and ease previously unavailable in programmable devices.

ACT 1 Family Three-State Procedure

Three-stating an ACT 1 device is easy using the unique debugging features of the Actel architecture. Three special pins on Actel devices are used for this function: MODE, SDI, and DCLK. To maintain the three-stating feature on ACT 1 devices, no user-defined output or bidirectional pins may be assigned to the SDI and DCLK locations. These pins should remain unassigned or should be defined as input-only locations. All other user-defined pins have no restrictions for their function; they may be assigned as input-only, output-only, or bidirectional pins. These pins can be temporarily three-stated for testing and debugging.

Figure 1 shows the sequence for three-stating an ACT 1 device. Seven data bits are clocked into the device using the SDI pin as data input and DCLK as the clock signal. The MODE pin distinguishes “test” mode from “normal” mode. The data sequence is {0001011}. After clocking the seventh bit, all user-defined pins are placed in a three-state condition until MODE is returned to logic low.

ACT 2, 1200XL, 3200DX, and ACT 3 Families Three-State Procedure

The same special purpose pins are used to three-state ACT 2, 1200XL, 3200DX, and ACT 3 devices: MODE, SDI, and DCLK. In contrast to the ACT 1 family, there are no restrictions on the assignment of user-defined functions to these pins. All user-defined pins have no restrictions for their function; they may be assigned as input-only, output-only, or bidirectional pins.

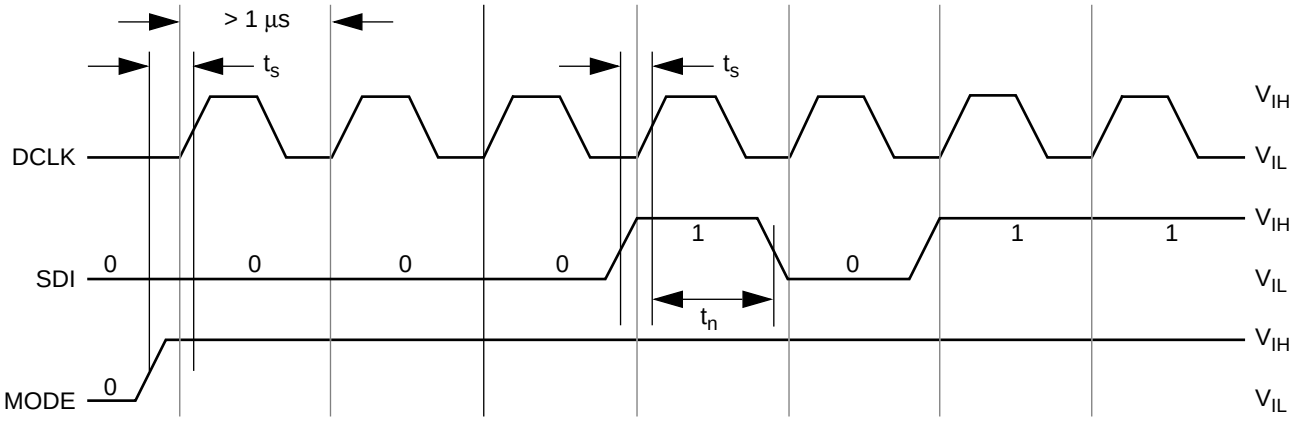
Thirty-two data bits are clocked into the device using the SDI pin as data input and DCLK as the clock signal. The MODE pin distinguishes “test” mode from “normal” mode. The data sequence for ACT 2, 1200XL, 3200DX, and ACT 3 devices is determined by the programmed state of the device. For unprogrammed, blank devices, the data sequence is

(LSB) 0000000000 0000000000 0000000111 10 (MSB)

For programmed devices, the data sequence is

(LSB) 0000000000 0000000000 0000000110 00 (MSB)

Load the data beginning with the LSB. After clocking the 32nd bit, all user-defined pins are placed in a three-state condition until MODE is returned to logic low. Use the same relative timing for the MODE, SDI, and DCLK inputs as shown in Figure 1.



Notes:

1. *$0\ V \le V_{IL} \le 0.5\ V;\ 3.0\ V \le V_{IH} \le VCC$*
2. *Test mode configuration is a low frequency (< 1.0 MHz) operation.*
3. *All setup and hold conditions (t_n, t^s) ≥ 250 ns.*

Figure 1 • *ACT 1 Device Three-State Timing Diagram*